IBM Field Engineering Handbook

Restricted Distribution

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System/360, General Section

Y22-2851-0

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Y22-2851-0

Fourth Edition (August 1968)
This is a major revision of, and obsoletes, Z22-2851-2. This publication has been entirely rewritten to reflect numerous additions and changes, and it should be reviewed in its entirety. Changes are periodically made to the specifications herein; any such changes will be reported in subsequent revisions or FE Supplements.

This publication has been prepared by the IBM Systems Development Division, Field Engineering Technical Operations, Dept. 900, PO Box 390, Poughkeepsie, New York 12602. A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be sent to the above address.

CE SAFETY PRACTICES

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
2. Remove all power AC and DC when removing or assembling major components, working in immediate area of power supplies, performing mechanical inspection of power supplies and installing changes in machine circuitry.
3. Wall box power switch when turned off should be locked or tagged in off position. "Do not Operate" tags, form 229-1266, affixed when applicable. Pull power supply cord whenever possible.
4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, the following precautions must be followed:
   a. Another person familiar with power off controls must be in immediate vicinity.
   b. Rings, wrist watches, chains, bracelets, metal cuff links, shall not be worn.
   c. Only insulated pliers and screwdrivers shall be used.
   d. Keep one hand in pocket.
   e. When using test instruments be certain controls are set correctly and proper capacity, insulated probes are used.
   f. Avoid contacting ground potential (metal floor strips, machine frames, etc. — use suitable rubber mats purchased locally if necessary).
5. Safety Glasses must be worn when:
   a. Using a hammer to drive pins, riveting, staking, etc.
   b. Power hand drilling, reaming, grinding, etc.
   c. Using spring hooks, attaching springs.
   d. Soldering, wire cutting, removing steel bands.
   e. Parts cleaning, using solvents, sprays, cleaners, chemicals, etc.
   f. All other conditions that may be hazardous to your eyes. REMEMBER, THEY ARE **YOUR** EYES.
6. Special safety instructions such as handling Cathode Ray Tubes and extreme high voltages, must be followed as outlined in CEM's and Safety Section of the Maintenance Manuals.
7. Do not use solvents, chemicals, greases or oils that have not been approved by IBM.
8. Avoid using tools or test equipment that have not been approved by IBM.
9. Replace worn or broken tools and test equipment.
10. Lift by standing or pushing up with stronger leg muscles — this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
11. All safety devices such as guards, shields, signs, ground wires, etc. shall be restored after maintenance.

KNOWING SAFETY RULES IS NOT ENOUGH

AN UNSAFE ACT WILL INEVITABLY LEAD TO AN ACCIDENT

USE GOOD JUDGMENT — ELIMINATE UNSAFE ACTS

229-1264-1

12. Each Customer Engineer is responsible to be certain that no action on his part renders product unsafe or exposes hazards to customer personnel.
13. Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
14. All machine covers must be in place before machine is returned to customer.
15. Always place CE tool kit away from walk areas where no one can trip over it (i.e., under desk or table).
16. Avoid touching mechanical moving parts (i.e., when lubricating, checking for play, etc.).
17. When using stroboscope — do not touch ANYTHING — it may be moving.
18. Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
19. Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
20. Before starting equipment, make certain fellow CE's and customer personnel are not in a hazardous position.
21. Maintain good housekeeping in area of machines while performing and after completing maintenance.

Artificial Respiration

GENERAL CONSIDERATIONS

1. **Start Immediately, Seconds Count**
   Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim or apply stimulants.
2. **Check Mouth for Obstructions**
   Remove foreign objects — Pull tongue forward.
3. **Loosen Clothing — Keep Warm**
   Take care of these items after victim is breathing by himself or when help is available.
4. **Remain in Position**
   After victim revives, be ready to resume respiration if necessary.
5. **Call a Doctor**
   Have someone summon medical aid.
6. **Don't Give Up**
   Continue without interruption until victim is breathing without help or is certainly dead.

Reprint Courtesy Mine Safety Appliances Co.

Rescue Breathing for Adults
Victim on His Back Immediately

1. **Clear throat** of water, food, or foreign matter.
2. **Tilt head back** to open air passage.
3. **Lift jaw up** to keep tongue out of air passage.
4. **Pinch nostrils** to prevent air leakage when you blow.
5. Blow until you see chest rise.
6. **Remove your lips** and allow lungs to empty.
7. **Listen** for snoring and gurglings, signs of throat obstruction.
8. **Repeat mouth to mouth breathings** 10-20 times a minute.

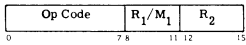
Continue rescue breathing until he breathes for himself.

Thumb and finger positions

Final mouth to mouth position

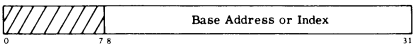
INSTRUCTION FORMATS

RR Format

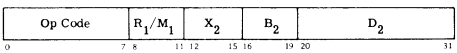


R1, R2 - Meaningful for all RR instructions except SPM and SVC

BASE AND INDEX REGISTERS



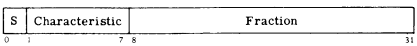
RX Format



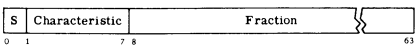
R1, D2(X2, B2)
R1, S2(X2)

R1, D2(0, B2)
R1, S2

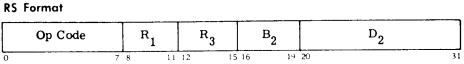
SHORT FLOATING-POINT NUMBER



LONG FLOATING-POINT NUMBER



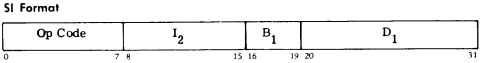
RS Format



R1, R3, D2(B2) } BXH, BXLE,
R1, R3, S2 } LM, STM

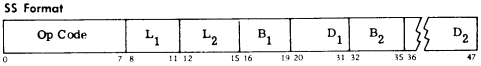
R1, D2(B2) } Shift
R1, S2 } instructions

SI Format



D1(B1) LPSW, SSM, HIO, SIO
S1 TIO, TCH, TS
D1(B1), I2 } All other SI Instructions
S1, I2 }

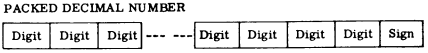
SS Format



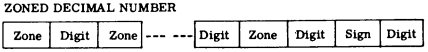
D1(L1, B1), D2(L2, B2) } PACK, UNPK, MVO, AP,
S1(L1), S2(L2) } CP, DP, MP, SP, ZAP

D1(L, B1), D2(B2) } NC, OC, XC, CLC, MVC, MVN,
S1(L), S2 } MVZ, TR, TRT, ED, EDMK

PACKED DECIMAL NUMBER



ZONED DECIMAL NUMBER



RR FORMAT INSTRUCTIONS

Standard Instruction Set

Floating-Point Feature Instructions

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
0	00					12-0-1-8-9	0000 0000	ccw
1	01					12-1-9	0000 0001	
2	02					12-2-9	0000 0010	
3	03					12-3-9	0000 0011	
4	04	SPM		PF		12-4-9	0000 0100	
5	05	BALR		HT		12-5-9	0000 0101	
6	06	BCTR		LC		12-6-9	0000 0110	
7	07	BCR		DEL		12-7-9	0000 0111	
8	08	SSK				12-8-9	0000 1000	ccw
9	09	ISK				12-1-8-9	0000 1001	
10	0A	SVC				12-2-8-9	0000 1010	
11	0B					12-3-8-9	0000 1011	
12	0C	(EBCDIC +)				12-4-8-9	0000 1100	
13	0D	(EBCDIC −)				12-5-8-9	0000 1101	
14	0E					12-6-8-9	0000 1110	
15	0F			CU1		12-7-8-9	0000 1111	
16	10	LPR				12-11-1-8-9	0001 0000	ccw
17	11	LNR				11-1-9	0001 0001	
18	12	LTR				11-2-9	0001 0010	
19	13	LCR				11-3-9	0001 0011	
20	14	NR		RES		11-4-9	0001 0100	
21	15	CLR		NL		11-5-9	0001 0101	
22	16	OR		BS		11-6-9	0001 0110	
23	17	XR		IL		11-7-9	0001 0111	
24	18	LR				11-8-9	0001 1000	ccw
25	19	CR				11-1-8-9	0001 1001	
26	1A	AR		CC		11-2-8-9	0001 1010	
27	1B	SR				11-3-8-9	0001 1011	
28	1C	MR				11-4-8-9	0001 1100	
29	1D	DR				11-5-8-9	0001 1101	
30	1E	ALR				11-6-8-9	0001 1110	
31	1F	SLR		CU2		11-7-8-9	0001 1111	
32	20	LPDR				11-0-1-8-9	0010 0000	ccw
33	21	LNDR				0-1-9	0010 0001	
34	22	LTDR				0-2-9	0010 0010	
35	23	LCDR				0-3-9	0010 0011	
36	24	HDR		BYP		0-4-9	0010 0100	
37	25	LRDR		LF		0-5-9	0010 0101	
38	26	MXR		EOB		0-6-9	0010 0110	
39	27	MXDR		PRE		0-7-9	0010 0111	
40	28	LDR				0-8-9	0010 1000	ccw
41	29	CDR				0-1-8-9	0010 1001	
42	2A	ADR		SM		0-2-8-9	0010 1010	
43	2B	SDR				0-3-8-9	0010 1011	
44	2C	MDR				0-4-8-9	0010 1100	
45	2D	DDR				0-5-8-9	0010 1101	
46	2E	AWR				0-6-8-9	0010 1110	
47	2F	SWR		CU3		0-7-8-9	0010 1111	
48	30	LPER				12-11-0-1-8-9	0011 0000	ccw
49	31	LNER				1-9	0011 0001	
50	32	LTER				2-9	0011 0010	
51	33	LCER				3-9	0011 0011	
52	34	HER		PN		4-9	0011 0100	
53	35	LRER		RS		5-9	0011 0101	
54	36	AXR		UC		6-9	0011 0110	
55	37	SXR		EOT		7-9	0011 0111	
56	38	LER				8-9	0011 1000	ccw
57	39	CER				1-8-9	0011 1001	
58	3A	AER				2-8-9	0011 1010	
59	3B	SER				3-8-9	0011 1011	
60	3C	MER				4-8-9	0011 1100	
61	3D	DER				5-8-9	0011 1101	
62	3E	AUR				6-8-9	0011 1110	
63	3F	SUR				7-8-9	0011 1111	

(2) Note that check bit (C) is not shown; add C bit for odd or even parity as needed except for even parity, decimal 64 is CA, the same as decimal 122
(3) CCW flag bit assignments
(4) Decimal feature instructions
(5) System/360 assembler programs require these codes

Standard Instruction Set

Floating-Point Feature Instructions

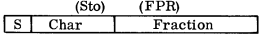
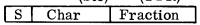
Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)	(5)
64	40	STH		SP	(2)	no punches	0100 0000	CCW	
65	41	LA				12-0-1-9	0100 0001		
66	42	STC				12-0-2-9	0100 0010		
67	43	IC				12-0-3-9	0100 0011		
68	44	EX				12-0-4-9	0100 0100		
69	45	BAL				12-0-5-9	0100 0101		
70	46	BCT				12-0-6-9	0100 0110		
71	47	BC				12-0-7-9	0100 0111		
72	48	LH				12-0-8-9	0100 1000	CCW	
73	49	CH				12-1-8	0100 1001		
74	4A	AH		¢		12-2-8	0100 1010		
75	4B	SH	.	.	B A 8 2 1	12-3-8	0100 1011		
76	4C	MH	‡)	<	B A 8 4	12-4-8	0100 1100		
77	4D		[	(	B A 8 4 1	12-5-8	0100 1101		(
78	4E	CVD	<	+	B A 8 4 2	12-6-8	0100 1110		+
79	4F	CVB	≠	!	B A 8 4 2 1	12-7-8	0100 1111		
80	50	ST	& +	&	B A	12	0101 0000	CCW	
81	51					12-11-1-9	0101 0001		
82	52					12-11-2-9	0101 0010		
83	53					12-11-3-9	0101 0011		
84	54	N				12-11-4-9	0101 0100		
85	55	CL				12-11-5-9	0101 0101		
86	56	O				12-11-6-9	0101 0110		
87	57	X				12-11-7-9	0101 0111		
88	58	L				12-11-8-9	0101 1000	CCW	
89	59	C				11-1-8	0101 1001		
90	5A	A		!		11-2-8	0101 1010		
91	5B	S	$	$	B 8 2 1	11-3-8	0101 1011		
92	5C	M	*	*	B 8 4	11-4-8	0101 1100		
93	5D	D	]	)	B 8 4 1	11-5-8	0101 1101		)
94	5E	AL	;	;	B 8 4 2	11-6-8	0101 1110		
95	5F	SL	Δ	¬	B 8 4 2 1	11-7-8	0101 1111		
96	60	STD	-	-	B	11	0110 0000	CCW	
97	61		/	/	A 1	0-1	0110 0001		
98	62					11-0-2-9	0110 0010		
99	63					11-0-3-9	0110 0011		
100	64					11-0-4-9	0110 0100		
101	65					11-0-5-9	0110 0101		
102	66					11-0-6-9	0110 0110		
103	67	MXD				11-0-7-9	0110 0111		
104	68	LD				11-0-8-9	0110 1000	CCW	
105	69	CD				0-1-8	0110 1001		
106	6A	AD				12-11	0110 1010		
107	6B	SD	,	,	A 8 2 1	0-3-8	0110 1011		
108	6C	MD	% (	%	A 8 4	0-4-8	0110 1100		
109	6D	DD	∨	—	A 8 4 1	0-5-8	0110 1101		
110	6E	AW	\	>	A 8 4 2	0-6-8	0110 1110	\	
111	6F	SW	##	?	A 8 4 2 1	0-7-8	0110 1111		
112	70	STE				12-11-0	0111 0000	CCW	
113	71					12-11-0-1-9	0111 0001		
114	72					12-11-0-2-9	0111 0010		
115	73					12-11-0-3-9	0111 0011		
116	74					12-11-0-4-9	0111 0100		
117	75					12-11-0-5-9	0111 0101		
118	76					12-11-0-6-9	0111 0110		
119	77					12-11-0-7-9	0111 0111		
120	78	LE				12-11-0-8-9	0111 1000	CCW	
121	79	CE				1-8	0111 1001		
122	7A	AE	↑	:	A	2-8	0111 1010		
123	7B	SE	# =	#	8 2 1	3-8	0111 1011		
124	7C	ME	@	@	8 4	4-8	0111 1100		
125	7D	DE	:	'	8 4 1	5-8	0111 1101		'
126	7E	AU	>	=	8 4 2	6-8	0111 1110		=
127	7F	SU	✓	"	8 4 2 1	7-8	0111 1111		

Deci-mal	Hexa-deci-mal	Mnemonic	Graphic & Control Symbols BCDIC EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
128	80	SSM			12-0-1-8	1000 0000	ccw
129	81		a		12-0-1	1000 0001	
130	82	LPSW	b		12-0-2	1000 0010	
131	83	(Diagnose)	c		12-0-3	1000 0011	
132	84	WRD	d		12-0-4	1000 0100	
133	85	RDD	e		12-0-5	1000 0101	
134	86	BXH	f		12-0-6	1000 0110	
135	87	BXLE	g		12-0-7	1000 0111	
136	88	SRL	h		12-0-8	1000 1000	ccw
137	89	SLL	i		12-0-9	1000 1001	
138	8A	SRA			12-0-2-8	1000 1010	
139	8B	SLA			12-0-3-8	1000 1011	
140	8C	SRDL			12-0-4-8	1000 1100	
141	8D	SLDL			12-0-5-8	1000 1101	
142	8E	SRDA			12-0-6-8	1000 1110	
143	8F	SLDA			12-0-7-8	1000 1111	
144	90	STM			12-11-1-8	1001 0000	ccw
145	91	TM	j		12-11-1	1001 0001	
146	92	MVI	k		12-11-2	1001 0010	
147	93	TS	l		12-11-3	1001 0011	
148	94	NI	m		12-11-4	1001 0100	
149	95	CLI	n		12-11-5	1001 0101	
150	96	OI	o		12-11-6	1001 0110	
151	97	XI	p		12-11-7	1001 0111	
152	98	LM	q		12-11-8	1001 1000	ccw
153	99		r		12-11-9	1001 1001	
154	9A				12-11-2-8	1001 1010	
155	9B				12-11-3-8	1001 1011	
156	9C	SIO			12-11-4-8	1001 1100	
157	9D	TIO			12-11-5-8	1001 1101	
158	9E	HIO			12-11-6-8	1001 1110	
159	9F	TCH			12-11-7-8	1001 1111	
160	A0				11-0-1-8	1010 0000	ccw
161	A1				11-0-1	1010 0001	
162	A2		s		11-0-2	1010 0010	
163	A3		t		11-0-3	1010 0011	
164	A4		u		11-0-4	1010 0100	
165	A5		v		11-0-5	1010 0101	
166	A6		w		11-0-6	1010 0110	
167	A7		x		11-0-7	1010 0111	
168	A8		y		11-0-8	1010 1000	ccw
169	A9		z		11-0-9	1010 1001	
170	AA				11-0-2-8	1010 1010	
171	AB				11-0-3-8	1010 1011	
172	AC				11-0-4-8	1010 1100	
173	AD				11-0-5-8	1010 1101	
174	AE				11-0-6-8	1010 1110	
175	AF				11-0-7-8	1010 1111	
176	B0				12-11-0-1-8	1011 0000	ccw
177	B1				12-11-0-1	1011 0001	
178	B2				12-11-0-2	1011 0010	
179	B3				12-11-0-3	1011 0011	
180	B4				12-11-0-4	1011 0100	
181	B5				12-11-0-5	1011 0101	
182	B6				12-11-0-6	1011 0110	
183	B7				12-11-0-7	1011 0111	
184	B8				12-11-0-8	1011 1000	ccw
185	B9	LMP			12-11-0-9	1011 1001	
186	BA				12-11-0-2-8	1011 1010	
187	BB				12-11-0-3-8	1011 1011	
188	BC				12-11-0-4-8	1011 1100	
189	BD				12-11-0-5-8	1011 1101	
190	BE				12-11-0-6-8	1011 1110	
191	BF				12-11-0-7-8	1011 1111	

Deci-mal	Hexa-deci-mal	Mnemonic	Graphic & Control Symbols BCDIC	EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
192	C0		?		B A 8 2	12-0	1100 0000	ccw
193	C1		A	A	B A 1	12-1	1100 0001	
194	C2		B	B	B A 2	12-2	1100 0010	
195	C3		C	C	B A 2 1	12-3	1100 0011	
196	C4		D	D	B A 4	12-4	1100 0100	
197	C5		E	E	B A 4 1	12-5	1100 0101	
198	C6		F	F	B A 4 2	12-6	1100 0110	
199	C7		G	G	B A 4 2 1	12-7	1100 0111	
200	C8		H	H	B A 8	12-8	1100 1000	ccw
201	C9		I	I	B A 8 1	12-9	1100 1001	
202	CA					12-0-2-8-9	1100 1010	
203	CB					12-0-3-8-9	1100 1011	
204	CC					12-0-4-8-9	1100 1100	
205	CD					12-0-5-8-9	1100 1101	
206	CE					12-0-6-8-9	1100 1110	
207	CF					12-0-7-8-9	1100 1111	
208	D0		!		B 8 2	11-0	1101 0000	ccw
209	D1	MVN	J	J	B 1	11-1	1101 0001	
210	D2	MVC	K	K	B 2	11-2	1101 0010	
211	D3	MVZ	L	L	B 2 1	11-3	1101 0011	
212	D4	NC	M	M	B 4	11-4	1101 0100	
213	D5	CLC	N	N	B 4 1	11-5	1101 0101	
214	D6	OC	O	O	B 4 2	11-6	1101 0110	
215	D7	XC	P	P	B 4 2 1	11-7	1101 0111	
216	D8		Q	Q	B 8	11-8	1101 1000	ccw
217	D9		R	R	B 8 1	11-9	1101 1001	
218	DA					12-11-2-8-9	1101 1010	
219	DB					12-11-3-8-9	1101 1011	
220	DC	TR				12-11-4-8-9	1101 1100	
221	DD	TRT				12-11-5-8-9	1101 1101	
222	DE	ED (4)				12-11-6-8-9	1101 1110	
223	DF	EDMK (4)				12-11-7-8-9	1101 1111	
224	E0		+		A 8 2	0-2-8	1110 0000	ccw
225	E1					11-0-1-9	1110 0001	
226	E2		S	S	A 2	0-2	1110 0010	
227	E3		T	T	A 2 1	0-3	1110 0011	
228	E4		U	U	A 4	0-4	1110 0100	
229	E5		V	V	A 4 1	0-5	1110 0101	
230	E6		W	W	A 4 2	0-6	1110 0110	
231	E7		X	X	A 4 2 1	0-7	1110 0111	
232	E8		Y	Y	A 8	0-8	1110 1000	ccw
233	E9		Z	Z	A 8 1	0-9	1110 1001	
234	EA					11-0-2-8-9	1110 1010	
235	EB					11-0-3-8-9	1110 1011	
236	EC					11-0-4-8-9	1110 1100	
237	ED					11-0-5-8-9	1110 1101	
238	EE					11-0-6-8-9	1110 1110	
239	EF					11-0-7-8-9	1110 1111	
240	F0		0	0	8 2	0	1111 0000	ccw
241	F1	MVO	1	1	1	1	1111 0001	
242	F2	PACK	2	2	2	2	1111 0010	
243	F3	UNPK	3	3	2 1	3	1111 0011	
244	F4		4	4	4	4	1111 0100	
245	F5		5	5	4 1	5	1111 0101	
246	F6		6	6	4 2	6	1111 0110	
247	F7		7	7	4 2 1	7	1111 0111	
248	F8	ZAP (4)	8	8	8	8	1111 1000	ccw
249	F9	CP (4)	9	9	8 1	9	1111 1001	
250	FA	AP (4)				12-11-0-2-8-9	1111 1010	
251	FB	SP (4)				12-11-0-3-8-9	1111 1011	
252	FC	MP (4)				12-11-0-4-8-9	1111 1100	
253	FD	DP (4)				12-11-0-5-8-9	1111 1101	
254	FE					12-11-0-6-8-9	1111 1110	
255	FF					12-11-0-7-8-9	1111 1111	

Condition Code Setting	0	1	2	3
Mask Bit Position	8	4	2	1
FLOATING-POINT ARITHMETIC				
Add Normalized S/L	zero	<zero	>zero	– –
Add Unnormalized S/L	zero	<zero	>zero	– –
Compare S/L (A:B)	equal	A low	A high	– –
Load and Test S/L	zero	<zero	>zero	– –
Load Complement S/L	zero	<zero	>zero	– –
Load Negative S/L	zero	<zero	– –	– –
Load Positive S/L	zero	– –	>zero	– –
Subtract Normalized S/L	zero	<zero	>zero	– –
Subtract Unnormalized S/L	zero	<zero	>zero	– –
FIXED-POINT ARITHMETIC				
Add H/F	zero	<zero	>zero	overflow
Add Logical	zero, no carry	not zero, no carry	zero, carry	not zero, carry
Compare H/F (A:B)	equal	A low	A high	– –
Load and Test	zero	<zero	>zero	– –
Load Complement	zero	<zero	>zero	overflow
Load Negative	zero	<zero	– –	– –
Load Positive	zero	– –	>zero	overflow
Shift Left Double	zero	<zero	>zero	overflow
Shift Left Single	zero	<zero	>zero	overflow
Shift Right Double	zero	<zero	>zero	– –
Shift Right Single	zero	<zero	>zero	– –
Subtract H/F	zero	<zero	>zero	overflow
Subtract Logical	– –	not zero, no carry	zero, carry	not zero, carry
DECIMAL ARITHMETIC				
Add Decimal	zero	<zero	>zero	overflow
Compare Decimal (A:B)	equal	A low	A high	– –
Subtract Decimal	zero	<zero	>zero	overflow
Zero and Add	zero	<zero	>zero	overflow
LOGICAL OPERATIONS				
AND	zero	not zero	– –	– –
Compare Logical (A:B)	equal	A low	A high	– –
Edit	zero	<zero	>zero	– –
Edit and Mark	zero	<zero	>zero	– –
Exclusive OR	zero	not zero	– –	– –
OR	zero	not zero	– –	– –
Test Under Mask	zero	mixed	– –	one
Translate and Test	zero	incomplete	complete	– –
STATUS SWITCHING				
Test and Set	zero	one	– –	– –
INPUT/OUTPUT OPERATIONS				
Halt I/O	not working	halted	stopped	not oper
Start I/O	available	CSW stored	busy	not oper
Test Channel	not working	CSW ready	working	not oper
Test I/O	available	CSW stored	working	not oper

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Add	A	5A	RX	R1, D2(X2, B2)	Add opr 2 to opr 1 (Sto) (Reg)	Adr Prot Spec Fxpt Oflo	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add	AR	1A	RR	R1, R2	Add opr 2 to opr 1 (GPR) (Reg)	Fxpt Oflo	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add Decimal	AP	FA	SS	D1, (L1, B1), D2(L2, B2)	Add dec opr 2 to opr 1 (Sto) (Sto) (Right to left byte by byte). (Opr 1 and 2 must be in packed) (Fields can overlap if low-order bytes coincide) (If opr 1 and opr 2 refer to same field, the field is doubled)	Prot Adr Data Dec Oflo Oper	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add Halfword	AH	4A	RX	R1, D2(X2, B2)	Add opr 2 to opr 1 (Sto) (Reg) (High-order 16 bits expanded) opr 2	Adr Spec Fxpt Oflo Prot	0 Sum = 0 1 Sum < 0 2 Sum > 0 3 Overflow
Add Logical	AL	5E	RX	R1, D2(X2, B2)	Add log opr 2 to opr 1 (Sto) (Reg)	Adr Spec Prot	0 Sum = 0 1 Sum ≠ 0 2 Sum = 0 3 Sum ≠ 0
Add Logical	ALR	1E	RR	R1, R2	Add log opr 2 to opr 1 (Reg) (Reg)		0 Sum = 0 1 Sum ≠ 0 2 Sum = 0 3 Sum ≠ 0

Add Normalized (Extended)	AXR	36	RR	R1, R2	FP Add opr 2 to opr 1 (FPR pair) (FPR pair) Extended sum is put in opr 1 (FPR pair) Each operand consists of two FPR Only FPR 0 and FPR 4 may be specified for opr 1 or opr 2.	Oper Spec Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Normalized (Long)	AD	6A	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR)  	Adr Oper Prot Spec Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Normalized (Long)	ADR	2A	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR)	Spec Oper Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Normalized (Short)	AE	7A	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR)  (Low-order halves of FPR ignored and unchanged)	Adr Prot Oper Spec Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Normalized (Short)	AER	3A	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR) (Low-order halves of FPR ignored and unchanged)	Spec Oper Sign Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Add Unnormalized (Long)	AW	6E	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR)	Adr Prot Oper Spec Sign Exp Oflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Unnormalized (Long)	AWR	2E	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR)	Spec Sign Exp Oflo Oper	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Unnormalized (Short)	AU	7E	RX	R1, D2(X2, B2)	FP Add opr 2 to opr 1 (Sto) (FPR) (Low-order halves of FPR ignored and unchanged)	Adr Prot Oper Spec Sign Exp Oflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
Add Unnormalized (Short)	AUR	3E	RR	R1, R2	FP Add opr 2 to opr 1 (FPR) (FPR) (Low-order halves of FPR ignored and unchanged)	Spec Sign Exp Oflo Oper	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --
AND	N	54	RX	R1, D2(X2, B2)	Place the product of both opr's into opr 1	Adr Prot Spec	0 Result = 0 1 Result ≠ 0
AND	NC	D4	SS	D1(L, B1), D2(B2)	Place the product of both opr's into opr 1 (Left to right byte by byte) (Max number of bytes ANDed: 256)	Prot Adr	0 Result = 0 1 Result ≠ 0
AND	NR	14	RR	R1, R2	Place the product of both opr's into opr 1	None	0 Result = 0 1 Result ≠ 0
AND	NI	94	SI	D1(B1), I2	AND the 1 byte from the instruction stream (8-15) to opr 1	Prot Adr	0 Result = 0 1 Result ≠ 0

Branch and Link	BAL	45	RX	R1, D2(X2, B2)	Store PSW 32-63 in opr 1 Branch to adr of opr 2 (If opr 2 = 0) Store, No Branch	None	Unchanged
Branch and Link	BALR	05	RR	R1, R2	Store PSW 32-63 in opr 1 Branch to adr of opr 2 (If opr 2 = 0) Store, No Branch	None	Unchanged
Branch on Condition	BC	47	RX	M1, D2(X2, B2)	Compare opr 1 with cond code (Mask) 8-11 (Mask = 7) Branch on non-zero cond code (Mask = 15) Uncond branch (Mask = 8) Cond code 00 (Mask = 4) Cond code 01 (Mask = 2) Cond code 10 (Mask = 1) Cond code 11 (NOP if cond not met)	None	Unchanged
Branch on Condition	BCR	07	RR	M1, R2	Compare opr 1 with cond code Branch to opr 2 adr if cond met (If opr 2 = 0) NOP	None	Unchanged
Branch on Count	BCT	46	RX	R1, D2(X2, B2)	Reduce opr 1 by 1 and branch to opr 2 adr (If opr 1 = 1) Reduce, No Branch (If opr 2 = 0) Reduce, No Branch	None	Unchanged
Branch on Count	BCTR	06	RR	R1, R2	Reduce opr 1 by 1 and branch to opr 2 adr (If opr 1 = 1) Reduce, No Branch (If opr 2 = 0) Reduce, No Branch	None	Unchanged
Branch on Index High	BXH	86	RS	R1, R3, D2(B2)	Add opr 3 to opr 1 Sum compared to opr 3 if opr 3 adr is odd Sum compared to opr 3 + 1 if opr 3 adr is even Branch to opr 2 adr if sum > opr 3/opr 3 + 1	None	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Branch on Index Low or Equal	BXLE	87	RS	R1, R3, D2(B2)	Same as Branch On Index High Branch to opr 2 adr if sum < or = opr 3 + 1	None	Unchanged
Compare	C	59	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (Reg)	Adr Spec Prot	0 opr's = 1 1st < 2 1st >
Compare	CR	19	RR	R1, R2	Compare opr 1 algebraically to opr 2	None	0 opr's = 1 1st < 2 1st >
Compare Decimal	CP	F9	SS	D1 (L1, B1), D2(L2, B2)	Compare opr 1 to opr 2 (binary right to left) byte by byte (Opr's must be packed) (Fields can overlap if low-order bytes coincide) (The shorter opr is extended with high-order zeros)	Adr Data Oper Prot	0 opr's = 1 1st < 2 1st >
Compare Halfword	CH	49	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (Hi-order 16 bits expanded) opr 2	Adr Spec Prot	0 opr's = 1 1st < 2 1st >
Compare Logical	CL	55	RX	R1, D2(X2, B2)	Compare opr 1 to opr 2 (binary left to right) (Terminates if/when ≠ found)	Adr Spec Prot	0 opr's = 1 1st < 2 1st >
Compare Logical	CLC	D5	SS	D1(L, B1), D2(B2)	Compare opr 1 to opr 2 (binary left to right) (Terminated if/when ≠ found) (opr length max 256 bytes)	Adr Prot	0 opr's = 1 1st < 2 1st >
Compare Logical	CLI	95	SI	D1(B1), I2	Compare opr 1 to opr 2 (Imm) (Sto) (binary left to right) (Terminates if/when ≠ found)	Adr Prot	0 opr's = 1 1st < 2 1st >

Compare Logical	CLR	15	RR	R1, R2	Compare opr 1 to opr 2 (binary left to right) (Terminates if/when ≠ found)	None	0 opr's = 1 1st < 2 1st >
Compare (Long)	CD	69	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (Equalize and subtract)	Adr Spec Oper Prot	0 opr's = 1 1st < 2 1st >
Compare (Long)	CDR	29	RR	R1, R2	Compare opr 1 algebraically to opr 2 (FPR) (Equalize and subtract)	Spec Oper	0 opr's = 1 1st < 2 1st >
Compare (Short)	CE	79	RX	R1, D2(X2, B2)	Compare opr 1 algebraically to opr 2 (FPR) (Sto) (Low-order halves of FPR ignored and unchanged)	Adr Spec Oper Prot	0 opr's = 1 1st < 2 1st >
Compare (Short)	CER	39	RR	R1, R2	Compare opr 1 algebraically to opr 2 (FPR) (FPR) (Low-order halves of FPR ignored and unchanged)	Spec Oper	0 opr's = 1 1st < 2 1st >
Convert to Binary	CVB	4F	RX	R1, D2(X2, B2)	Convert opr 2 (packed decimal) (Doubleword bounds) to binary and put in opr 1 location	Adr Prot Spec Data Fxpt Div	Unchanged
Convert to Decimal	CVD	4E	RX	R1, D2(X2, B2)	Convert opr 1 (binary) to packed decimal (doubleword bounds) and put in opr 2	Prot Adr Spec	Unchanged
Diagnose	---	83	SI	See Principles of Operation, Form A22-6821	See Principles of Operation, Form A22-6821	Priv Oper Prot Spec Adr	Unpredict-able

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Divide	D	5D	RX	R1, D2 (X2, B2)	Divide opr 1 by opr 2 (even and odd regs) (Sto) Opr 1 becomes quotient and remainder	Adr Prot Spec Fxpt Div	Unchanged
Divide	DR	1D	RR	R1, R2	Divide opr 1 by opr 2 Dividend: even and odd pair regs Opr 1 becomes quotient and remainder (full word only)	Spec Fxpt Div	Unchanged
Divide Decimal	DP	FD	SS	D1(L1, B1), D2(L2, B2)	Divide opr 1 by opr 2 Opr 1 becomes quotient and remainder (left justified) Dividend: at least 1 leading zero, max size 31 digits and sign Divisor: max size 15 digits and sign, numerically larger than dividend Both opr's packed format Remainder size = divisor size (Fields can overlap if low-order bytes coincide.)	Prot Adr Spec Data Dec Div Oper	Unchanged
Divide (Long)	DD	6D	RX	R1, D2(X2, B2)	FP Divide opr 1 by opr 2 (FPR) (Sto) Opr 1 becomes quotient (prenormalized)	Adr Spec Exp Oflo FP Div Oper Prot Exp Uflo	Unchanged
Divide (Long)	DDR	2D	RR	R1, R2	FP Divide opr 1 by opr 2 Prenormalize (FPR) (FPR) (Dividend) (Divisor) Opr 1 becomes quotient	Spec Oper Exp Oflo Exp Uflo FP Div	Unchanged

Divide (Short)	DE	7D	RX	R1, D2(X2, B2)	FP Divide opr 1 by opr 2 Prenormalize (Dividend) (Divisor) Opr 1 becomes quotient (Low-order halves of FPR ignored and unchanged)	Adr Oper Prot Spec Exp Oflo Exp Uflo FP Div	Unchanged
Divide (Short)	DER	3D	RR	R1, R2	FP Divide opr 1 by 2 Prenormalize (FPR) (FPR) (Dividend) (Divisor) Opr 1 becomes quotient (Low-order halves of FPR ignored and unchanged)	Spec Exp Oflo FP Div Oper Exp Uflo	Unchanged
Edit	ED	DE	SS	D1(L, B1), D2(B2)	Opr 1 = pattern, opr 2 = source Opr 2 is changed from packed to zoned and edited under control of opr 1. Opr's processed left to right (Fill char is 1st char in pattern field unless it is a digit/select/significance-start char.) (Opr 1 terminates operation) See Principles of Operation, Form A22-6821	Prot Adr Data Oper	Source 0 field = 0 1 field < 0 2 field > 0
Edit and Mark	EDMK	DF	SS	D1(L, B1), D2(B2)	Same as Edit (Adr of 1st significant result digit recorded in GPR 1)	Prot Adr Data Oper	Source 0 field = 0 1 field < 0 2 field > 0
Exclusive OR	X	57	RX	R1, D2(X2, B2)	Exclusive-OR opr 2 and opr 1 and the modulo-two sum placed in opr 1	Adr Spec Prot	0 Result = 0 1 Result ≠ 0

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Exclusive OR	XC	D7	SS	D1(L, B1), D2(B2)	Exclusive-OR opr 2 and opr 1 and the modulo-two sum placed in opr 1 (Left to right bit by bit) (Max opr length is 256 bytes)	Prot Adr	0 Result = 0 1 Result ≠ 0
Exclusive OR	XI	97	SI	D1(B1), I2	The 1 byte from the instruction stream (8-15) is exclusive-ORed with opr 1 and the modulo-two sum placed in opr 1	Prot Adr	0 Result = 0 1 Result ≠ 0
Exclusive OR	XR	17	RR	R1, R2	Exclusive-OR logical opr 2 and opr 1 and the modulo-two sum placed in opr 1.	None	0 Result = 0 1 Result ≠ 0
Execute	EX	44	RX	R1, D2(X2, B2)	Execute the instruction at the branch-to adr (modified by ORing target instruction 8-15 with opr 1 24-31) (If R1 - 0, execute - no ORing)	Execute Adr Spec Prot	Set by subject instruction
Halt I/O	HIO	9E	SI	D1(B1)	Current I/O operation of specified sub-channel or channel is terminated. (CSW 32-47 are stored) (Privileged instruction)	Priv Oper	0 Chan or sub-chan working 1 CSW stored 2 Burst oper terminated 3 Not operational
Halve (Long)	HDR	24	RR	R1, R2	Fraction of opr 2 shifted right 1, normalized, opr 2 placed in opr 1 (FPRs) (opr 2 unchanged)	Oper Spec Exp Uflo	Unchanged
Halve (Short)	HER	34	RR	R1, R2	Fraction of opr 2 shifted right 1, normalized, opr 2 placed in opr 1 (FPRs) (Low-order half of opr 1 unchanged, opr 2 unchanged)	Oper Spec Exp Uflo	Unchanged
Insert Character	IC	43	RX	R1, D2(X2, B2)	Opr 2's char placed into opr 1, 24-31 (High-order bits unchanged)	Adr Prot	Unchanged

Insert Storage Key	ISK	09	RR	R1, R2	Opr 2, 8-20 fetches 5-bit sto key byte. 5-bit sto key is placed in opr 1, 24-28. Bits 0-23 unchanged, 29-31 set to zero. (opr 2, 0-7 and 21-27 ignored, 28-31 must = 0) Opr 1 bit 28 set to 0 if fetch protect not installed.	Priv Oper Adr Spec	Unchanged
Load	L	58	RX	R1, D2(X2, B2)	Load opr 2 into opr 1	Spec Adr Prot	Unchanged
Load	LR	18	RR	R1, R2	Opr 2 into opr 1	None	Unchanged
Load Address	LA	41	RX	R1, D2(X2, B2)	Opr 2, 12-31 to opr 1, 8-31. Opr 1, 0-7 set to zero (no storage reference made)	None	Unchanged
Load and Test	LTR	12	RR	R1, R2	Opr 2 into opr 1 (When opr 1 and opr 2 specify same reg result is test without data transfer.)	None	0 Result = 0 1 Result < 0 2 Result > 0
Load and Test (Long)	LTDR	22	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (When opr 1 and opr 2 specify same reg result is test without data transfer.)	Spec Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0
Load and Test (Short)	LTER	32	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Low-order half of opr 1 unchanged) (When opr 1 and opr 2 specify same reg result is test without data transfer.)	Spec Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0
Load Complement	LCR	13	RR	R1, R2	2's complement of opr 2 into opr 1 (overflow when max negative number is complemented)	Fxpt Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Load Complement (Short)	LCER	33	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Opr 1 sign inverted, low-order half unchanged) (Opr 2 unchanged)	Spec Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0
Load Complement (Long)	LCDR	23	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Opr 1 sign inverted, low-order half unchanged) (Opr 2 unchanged) (Low-order half of opr 1 unchanged)	Same as LCER	Same as LCER
Load Halfword	LH	48	RX	R1, D2(X2, B2)	Opr 2 halfword expanded to fullword with sign bits, placed in opr 1 (High-order expanded)	Adr Spec Prot	Unchanged
Load (Long)	LD	68	RX	R1, D2(X2, B2)	Opr 2 into opr 1 (Sto) (FPR)	Adr Spec Prot Oper	Unchanged
Load (Long)	LDR	28	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR)	Spec Oper	Unchanged

Load Multiple	LM	98	RS	R1, R3, D2(B2)	Opr 2 into GPRs in ascending order Starting reg specified by opr 1, ending reg specified by opr 3 (Reg wrap-around possible)	Adr Spec Prot	Unchanged
Load Negative	LNR	11	RR	R1, R2	2's complement of opr 2 into opr 1 (Reg) (Reg) (If opr 2 contains a (-) number or zero, the number is unchanged)	None	0 Result = 0 1 Result < 0
Load Negative (Long)	LNDR	21	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) Opr 1 sign bit is 1 (negative) Opr 2 unchanged	Spec Oper	Result 0 Fract = 0 1 Result < 0
Load Negative (Short)	LNER	31	RR	R1, R2	Opr 2 into opr 1 Opr 1 sign bit is 1 (negative) Opr 2 unchanged (Low-order half of opr 1 unchanged)	Spec Oper	Result 0 Fract = 0 1 Result < 0
Load Positive	LPR	10	RR	R1, R2	Opr 2 into opr 1 (Negative numbers are complemented) (Overflow occurs when the max negative number is complemented)	Fxpt Oflo	0 Result = 0 2 Result > 0 3 Overflow
Load Positive (Long)	LPDR	20	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) Opr 1 sign bit made a zero (positive) Opr 2 unchanged	Spec Oper	Result 0 Fract = 0 2 Result > 0
Load Positive (Short)	LPER	30	RR	R1, R2	Opr 2 into opr 1 Opr 1 sign bit made a zero (positive) Opr 2 unchanged (Low-order half of opr 1 unchanged)	Spec Oper	Result 0 Fract = 0 2 Result > 0

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Load PSW	LSPW	82	SI	D1(B1)	Opr 1 into PSW (Opr 1 low-order 3 bit adr must = 0) (Instruction used to enter the problem or wait state)	Priv Oper Prot Adr Spec	Set by new PSW 34 and 35
Load (Short)	LE	78	RX	R1, D2(X2, B2)	Opr 2 into opr 1 (Sto) (FPR) (Low-order half of opr 1 unchanged)	Adr Spec Oper Prot	Unchanged
Load (Short)	LER	38	RR	R1, R2	Opr 2 into opr 1 (FPR) (FPR) (Low-order half of opr 1 unchanged)	Spec Oper	Unchanged
Load Rounded (Extended to Long)	LRDR	25	RR	R1, R2	Opr 2 is rounded from extended to long format and put in opr 1 (FPR pair) (FPR) Only FPR 0 and FPR 4 may be specified for opr 2.	Oper Spec Exp Oflo	Unchanged
Load Rounded (Long to Short)	LRER	35	RR	R1, R2	Opr 2 is rounded from long to short format and put into opr 1 (FPR) (FPR) Add an absolute 1 to opr 2, bit 32; carry will ripple left. Lower half of result FPR will remain unchanged.	Oper Spec Exp Oflo	Unchanged
Move	MVC	D2	SS	D1(L, B1), D2(B2)	Opr 2 to opr 1 (Left to right byte by byte) (Max number of bytes moved: 256) (No restriction on overlapping fields)	Prot Adr	Unchanged
Move	MVI	92	SI	D1(B1), I2	Move the 1 byte from the instruction stream (8-15) to opr 1	Prot Adr	Unchanged

Move Numerics	MVN	D1	SS	D1(L, B1), D2(B2)	The 4 low-order bits of opr 2 bytes into the 4 low-order bits of opr 1 bytes. (Left to right byte by byte) (Max number of bytes moved: 256) (High-order bits of each byte of both opr's unchanged.) (No restriction on overlapping fields.)	Prot Adr	Unchanged
Move with Offset	MVO	F1	SS	D1(L1, B1), D2(L2, B2)	Opr 2 to the left of and adjacent to the low-order 4 bits of opr 1. (Right to left byte by byte) (Data can be packed, unpacked, or binary format) (No restriction on overlapping fields) (Processing terminated by high-order bit in opr 1) (If opr 2 field shorter than opr 1, insert leading zeros in opr 2.)	Prot Adr	Unchanged
Move Zones	MVZ	D3	SS	D1(L, B1), D2(B2)	The 4 high-order bits of opr 2 bytes into the 4 high-order bits of opr 1 bytes (Left to right byte by byte) (Max number of bytes moved: 256) (Low-order bits of each byte of both opr's unchanged.) (No restriction on overlapping fields)	Prot Adr	Unchanged
Multiply	M	5C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 Product: even and odd pair regs Opr 1 becomes the product. (Opr 1 must specify an even-numbered reg) (Sign bit extended to 1st significant product digit)	Adr Spec Prot	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Multiply	MR	IC	RR	R1, R2	Multiply opr 1 by opr 2 Product: even and odd pair of regs Opr 1 becomes the product. (Opr 1 must specify an even-numbered reg) (Sign bit extended to 1st significant product digit)	Spec	Unchanged
Multiply (Extended)	MXR	26	RR	R1, R2	Multiply extended opr 1 by extended opr 2 (FPR pair) (FPR pair) Extended product is put in opr 1 (FPR pair) (Only FPR 0 and FPR 4 may be specified for either opr 1 or opr 2) (Low-order characteristic is made 14 < high-order characteristic except when the result would be > 0, then the low-order characteristic is made 128 > its correct value; sign of low-order characteristic remains the same as high-order characteristic)	Oper Spec Exp Oflo Exp Uflo	Unchanged
Multiply Decimal	MP	FC	SS	D1(L1,B1), D2(L2,B2)	Multiply opr 1 by opr 2 Multiplier: 8 bytes max size and shorter than the multiplicand. Multiplicand: must have high-order zeros equal to or greater than the size of the multiplier. (Both opr's in packed format) (Right to left byte by byte) Product: must contain at least 1 high-order zero.	Prot Adr Spec Data Oper	Unchanged

Multiply Halfword	MH	4C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 (Opr 2 is expanded to a 32-bit integer) (Only the low-order 32 bits of the product, opr 1, are retained)	Adr Spec Prot	Unchanged
Multiply (Long)	MD	6C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 (FPR) (Sto) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (15) = zero: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.)	Adr Spec Exp Oflo Exp Uflo Oper Prot	Unchanged
Multiply (Long)	MDR	2C	RR	R1, R2	Multiply opr 1 by opr 2 (FPR) (FPR) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (15) = 0: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.)	Spec Exp Oflo Exp Uflo Oper	Unchanged
Multiply (Long to Extended)	MXD	67	RX	R1, D2(X2, B2)	Multiply long opr 1 by long opr 2. (FPR) (Sto) Extended product is put in PFR pair specified by opr 1 (Only FPR 0 and FPR 4 may be specified for opr 1) (Signs of FPR pair are the same) (Can only use doubleword boundary in storage) (Continued)	Oper Prot Adr Spec Exp Oflo Exp Uflo	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Multiply (Long to Extended) (Cont'd)	MXD	67	RX	R1, D2(X2, B2)	(Low-order characteristic is made 14 < high-order characteristic except when the result would be > 0, then the low-order characteristic is made 128 > its correct value; sign of low-order characteristic remains the same as high-order characteristic)		
Multiply (Long to Extended)	MXDR	27	RR	R1, R2	Multiply long opr 1 by long opr 2. (FPR) (FPR) Extended product is put in FPR pair specified by opr 1 (Only FPR 0 and FPR 4 may be specified for opr 1) (Signs of FPR pair are the same) (Low-order characteristic is made 14 < high-order characteristic except when the result would be > 0, then the low-order characteristic is made 128 > its correct value; sign of low-order characteristic remains the same as the high-order characteristic)	Opr Spec Exp Oflo Exp Uflo	Unchanged
Multiply (Short)	ME	7C	RX	R1, D2(X2, B2)	Multiply opr 1 by opr 2 (FPR) (Sto) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (14) = 0: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.) (The 2 low-order fraction digits of the product always = zero.)	Adr Spec Exp Oflo Exp Uflo Oper Prot	Unchanged

Multiply (Short)	MER	3C	RR	R1, R2	Multiply opr 1 by opr 2 (FPR) (FPR) Product: prenormalizes the opr's and post-normalizes the intermediate product. (If all fraction digits (14) = 0: the product sign and char are made zero.) (The intermediate product fraction is truncated before left-shifting.)	Spec Exp Oflo Exp Uflo Oper	Unchanged
OR	O	56	RX	R1, D2(X2, B2)	The ORed sum of both opr's into opr 1	Adr Spec Prot	0 Result = 0 1 Result ≠ 0
OR	OC	D6	SS	D1(L, B1), D2(B2)	The ORed sum of both opr's into opr 1 (Left to right byte by byte) (Max number of bytes ORed: 256)	Prot Adr	0 Result = 0 1 Result ≠ 0
OR	OR	16	RR	R1, R2	The ORed sum of both opr's into opr 1	None	0 Result = 0 1 Result ≠ 0
OR	OI	96	SI	D1(B1), I2	OR the 1 byte from the instruction stream (8-15) to opr 1	Prot Adr	0 Result = 0 1 Result ≠ 0
Pack	PACK	F2	SS	D1(L1, B1), D2(L2, B2)	Change opr 2 from zoned to packed format and place into opr 1. (Right to left byte by byte) (No restriction on overlapping fields) (Opr 2 may be extended with hi-order zeros)	Prot Adr	Unchanged
Read Direct	RDD	85	SI	D1(B1), I2	The 1 byte from the instruction stream (8-15) is placed on the signal-out, in a form of 8 timing pulses, along with a 9th pulse at the read-out line. The 8 bit lines at the direct-in lines are stored in opr 1.	Priv Oper Prot Adr	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Set Program Mask	SPM	04	RR	R1	Opr 1 (2-7) replaces the cond code and program mask bits of the current PSW (34-39) (Bits 0, 1 and 8-31 of opr 1 are ignored and unchanged.)	None	Set by bits 2 and 3
Set Storage Key	SSK	08	RR	R1, R2	Opr 1 (24-28) replaces the storage key specified by opr 2 (Opr 1 bits 0-23 and 29-31 are ignored) (Opr 2 bits 0-7 and 21-27 are ignored) (Bits 28-31 must be zero)	Priv Oper Adr Spec	Unchanged
Set System Mask	SSM	80	SI	D1 (B1)	Opr 1 (1 byte) replaces the system mask bits of the current PSW (0-7).	Priv Adr Prot	Unchanged
Shift Left Double	SLDA	8F	RS	R1, D2(B2)	Opr 1 (even and odd regs) is shifted left the number of times equal to opr 2 (low-order 6 bits).	Spec Fxpt Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow
Shift Left Double Logical	SLDL	8D	RS	R1, D2(B2)	Opr 1 (even and odd regs) is shifted left the number of times equal to opr 2 (low-order 6 bits). (Hi-order bit participates in the shift)	Spec	Unchanged
Shift Left Single	SLA	8B	RS	R1, D2(B2)	Opr 1 is shifted left the number of times equal to opr 2 (low-order 6 bits).	Fxpt Oflo	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow
Shift Left Single Logical	SLL	89	RS	R1, D2(B2)	Opr 1 is shifted left the number of times equal to opr 2 (low-order 6 bits). (Hi-order bit participates in the shift)	None	Unchanged

Shift Right Double	SRDA	8E	RS	R1, D2(B2)	Opr 1 (even and odd regs) is shifted right the number of times equal to opr 2 (low-order 6 bits).	Spec	0 Result = 0 1 Result < 0 2 Result > 0
Shift Right Double Logical	SRDL	8C	RS	R1, D2(B2)	Opr 1 (even and odd regs) is shifted right the number of times equal to opr 2 (low-order 6 bits). (Vacated bits are replaced with zeros) (Hi-order bit participates in the shift)	Spec	Unchanged
Shift Right Single	SRA	8A	RS	R1, D2(B2)	Opr 1 is shifted right the number of times equal to opr 2 (low-order 6 bits). (Shifting (+) numbers: vacated bits are replaced with zeros.) (Shifting (-) numbers: vacated bits are replaced with ones.)	None	0 Result = 0 1 Result < 0 2 Result > 0
Shift Right Single Logical	SRL	88	RS	R1, D2(B2)	Opr 1 is shifted right the number of times equal to opr 2 (low-order 6 bits). (Vacated bits are replaced with zeros) (Hi-order bit participates in the shift)	None	Unchanged
Start I/O	SIO	9C	SI	D1(B1)	Opr 1 (16-31) identifies the selected chan, ctl unit and I/O device to perform write, read, read bkwd, control or sense oper. The CAW at loc 48 is fetched, which locates the first CCW. The SIO is initiated providing the addressed chan, ctl unit and I/O device are available without pending interrupt errors, exceptional conditions pending.	Priv Oper	0=I/O oper initiated and chan proceeding with operation 1=CSW stored 2=Chan or subchannel busy 3=Not operational
Store	ST	50	RX	R1, D2(X2, B2)	Opr 1 is stored into opr 2	Prot Adr Spec	Unchanged

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Store Character	STC	42	RX	R1, D2(X2, B2)	Opr 1 (24-31) replaces the character at opr 2's address.	Prot Adr	Unchanged
Store Halfword	STH	40	RX	R1, D2(X2, B2)	Opr 1 (16 low-order bits) is stored at opr 2's location. (Hi-order bits, opr 1, ignored and unchanged)	Adr Prot Spec	Unchanged
Store (Long)	STD	60	RX	R1, D2(X2, B2)	FP opr 1 to opr 2's location	Adr Prot Spec Oper	Unchanged
Store Multiple	STM	90	RS	R1, R3, D2(B2)	Opr 1 thru opr 3 are stored at opr 2's location in ascending order. Starting reg specified by opr 1, ending reg specified by opr 3. (Reg wrap-around possible)	Adr Prot Spec	Unchanged
Store (Short)	STE	70	RX	R1, D2(X2, B2)	FP opr 1 is stored at opr 2's location (Low-order half of FPR ignored and unchanged)	Adr Prot Spec Oper	Unchanged
Subtract	S	5B	RX	R1, D2(X2, B2)	Subtract opr 2 from opr 1 and place the difference into opr 1	Adr Spec Fxpt Oflo Prot	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract	SR	1B	RR	R1, R2	Subtract opr 2 from opr 1; difference placed into opr 1.	Fxpt Oflo	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow

Subtract Decimal	SP	FB	SS	D1(L1, B1), D2(L2, B2)	Subtract dec opr 2 from opr 1; difference stored into opr 1. (Right to left byte by byte) (Both opr's must be in packed format) (Fields can overlap if low-order bytes coincide)	Prot Adr Data Dec Oflo Oper	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract Halfword	SH	4B	RX	R1, D2(X2, B2)	Opr 2 halfword expanded to fullword and subtracted from opr 1; difference placed into opr 1.	Adr Spec Fxpt Oflo Prot	0 Dif = 0 1 Dif < 0 2 Dif > 0 3 Overflow
Subtract Logical	SL	5F	RX	R1, D2(X2, B2)	Subtract opr 2 from opr 1; difference placed into opr 1.	Adr Spec Prot	0 -- 1 Dif ≠ 0 No Carry 2 Dif = 0 Carry 3 Dif ≠ 0 Carry
Subtract Logical	SLR	1F	RR	R1, R2	Subtract opr 2 from opr 1; difference placed into opr 1.	None	0 -- 1 Dif ≠ 0 No Carry 2 Dif = 0 Carry 3 Dif ≠ 0 Carry
Subtract Normalized (Extended)	SXR	37	RR	R1, R2	FP subtract extended opr 2 from extended opr 1. (FPR pair) (FPR pair) Extended difference is put in opr 1 (FPR pair) (Sign of extended opr 2 is inverted before the addition) (Only FPR 0 and FPR 4 may be specified for either opr 1 or opr 2) (Continued)	Oper Spec Exp Oflo Exp Uflo	0 Fract = 0 1 Fract < 0 2 Fract > 0 3 --

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Subtract Normalized (Extended) (Cont'd)	SXR	37	RR	R1, R2	(High-order and low-order signs of a FPR pair are always the same in extended precision) (Low-order characteristic is made 14 < high-order characteristic except when the result would be > 0, then the low-order characteristic is made 128 > its correct value; sign of low-order characteristic remains the same as high-order characteristic)		
Subtract Normalized (Long)	SD	6B	RX	R1, D2(X2, B2)	FP Subtract opr 2 from opr 1 and the difference placed into opr 1. (The sign of opr 2 is inverted before the addition.)	Adr Spec Sign Exp Oflo Exp Uflo Prot Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 --
Subtract Normalized (Long)	SDR	2B	RR	R1, R2	FP Subtract opr 2 from opr 1 (FPR) (FPR) (The sign of opr 2 is inverted before the addition.)	Spec Sign Exp Oflo Exp Uflo Prot Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Normalized (Short)	SE	7B	RX	R1, D2(X2, B2)	FP Subtract opr 2 from opr 1 (The sign of opr 2 is inverted before the addition.) (Low-order halves of FPR ignored and unchanged)	Adr Spec Sign Exp Oflo Exp Uflo Prot Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo

Subtract Normalized (Short)	SER	3B	RR	R1, R2	Subtract opr 2 from opr 1 (The sign of opr 2 is inverted before the addition.) (Low-order halves of FPRs ignored and unchanged)	Spec Sign Exp Oflo Exp Uflo Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Long)	SW	6F	RX	R1, D2(X2, B2)	FP Subtract opr 2 from opr 1 (Sto) (FPR) (The sign of opr 2 is inverted before the addition.)	Adr Spec Sign Exp Oflo Oper Prot	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Long)	SWR	2F	RR	R1, R2	FP Subtract opr 2 from opr 1 (FPR) (FPR) (The sign of opr 2 is inverted before the addition.)	Spec Sign Exp Oflo Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Short)	SU	7F	RX	R1, D2(X2, B2)	FP Subtract opr 2 from opr 1 (Sto) (FPR) (Low-order half of FPR ignored and unchanged) (The sign of opr 2 is inverted before the addition.)	Adr Spec Sign Exp Oflo Oper Prot	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 Exp Oflo
Subtract Unnormalized (Short)	SUR	3F	RR	R1, R2	FP Subtract opr 2 from opr 1 (FPR) (FPR) (Low-order halves of FPRs ignored and unchanged) (The sign of opr 2 is inverted before the addition.)	Spec Sign Exp Oflo Oper	Result 0 Fract = 0 1 Result < 0 2 Result > 0 3 --

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Supervisor Call	SVC	OA	RR	I	Immediate bits (8-15) replace (24-31) of the old PSW which is stored as a result of the interrupt. (16-23) are made zero. (Old PSW at loc 32) (New PSW from loc 96)	None	Unchanged
Test and Set	TS	93	SI	D1(B1)	Hi-order bit of 1st byte of opr adr sets cond code. Entire byte then set to 1's	Prot Adr	0 Hi-order bit = 0 1 Hi-order bit = 1 2 -- 3 --
Test Channel	TCH	9F	SI	D1(B1)	Opr 1 (16-23) identifies the tested channel. (Bits 24-31 are ignored.) (Instruction checks the channel's status and sets appropriate cond code.)	Priv Oper	0 Chan Avl 1 Int Pending 2 Chan in Burst Mode 3 Chan not Operational
Test I/O	TIO	9D	SI	D1(B1)	Opr 1 (16-31) identifies the tested channel, control unit, and I/O device. Used to clear a pending interrupt. (CSW stored at loc 64): Subchannel contains a pending interrupt. I/O device contains a pending interrupt. Control unit or I/O device is executing a previous operation or a pending channel-end/control unit-end for another I/O device. Channel or I/O device equipment error or device not ready.	Priv Oper	0 Available 1 CSW Stored 2 Channel or Subchan Busy 3 Not Operational

Test Under Mask	TM	91	SI	D1(B1), I2	Immediate bits (8-15) used as a mask to compare against opr 1. Mask bit 1: storage bit tested. Mask bit 0: storage bit ignored.	Prot Adr	0 Selected bits all zero (mask is all zero) 1 Selected bits mixed 0's and 1's 3 Selected bits all 1's
Translate	TR	DC	SS	D1(L, B1), D2(B2)	Opr 1 (argument byte) added to the initial adr of opr 2 (24-31). This adr now is the loc of the function byte which replaces the original argument byte (left to right byte by byte) (All data is valid) (Oper is terminated when opr 1 field is exhausted)	Prot Adr	Unchanged
Translate and Test	TRT	DD	SS	D1(L, B1), D2(B2)	(Same as TR) When the function byte is a zero the next argument byte is translated. Both opr's remain unchanged. When the function byte is a non-zero the operation is completed. The generated argument adr is placed into GPR 1, 8-31. Bits 0-7 remain unchanged. The function byte is placed into GPR 2, 24-31. (Left to right byte by byte) Bits 0-23 remain unchanged. If opr 1 is exhausted before a non-zero cond, the opr is completed and GPRs 1 and 2 remain unchanged.	Adr Prot	0 All function bytes 0 1 Non-0 function byte met 2 Last function byte non-0 3 Not used

Operation	Mnemonic	Op Code	Format	Operands	Description	Interruptions	Cond Code
Unpack	UNPK	F3	SS	D1(L1, B1), D2(L2, B2)	Change opr 2 from packed to zoned format and place into opr 1. (Right to left byte by byte) (No restrictions on overlapping fields) (Opr 2 may be extended with hi-order zeros.) (If PSW bit 12 = 1) ASCII zone code (If PSW bit 12 = 0) EBCDIC zone code inserted	Adr Prot	Unchanged
Write Direct	WRD	84	SI	D1(B1), I2	The 1 byte from the instruction stream (8-15) is placed on the timing signal out, in a form of 8 timing pulses, along with a 9th pulse at the write-out line. The 8 bit lines at the direct-out lines are brought up by opr 1.	Priv Oper Adr Prot	Unchanged
Zero and Add	ZAP	F8	SS	D1(L1, B1), D2(L2, B2)	Opr 1 cleared and opr 2 placed in opr 1 (Low-order opr's may coincide) (Opr 2 must be in packed format) (Opr 1 field must be large enough for all opr 2 significant digits) (Opr 2 extended with zeros to fill opr 1.)	Prot Adr Data Dec Oflo Oper	0 Result = 0 1 Result < 0 2 Result > 0 3 Overflow

EXTENDED IBM CARD CODE TO HEXADECIMAL

Digits	Bl	T	E	O	TEO	TE	TO	EO
				(Zones)				
Bl	40	50	60	F0	70	6A	C0	D0
1	F1	C1	D1	61	B1	91	81	A1
2	F2	C2	D2	E2	B2	92	82	A2
3	F3	C3	D3	E3	B3	93	83	A3
4	F4	C4	D4	E4	B4	94	84	A4
5	F5	C5	D5	E5	B5	95	85	A5
6	F6	C6	D6	E6	B6	96	86	A6
7	F7	C7	D7	E7	B7	97	87	A7
8	F8	C8	D8	E8	B8	98	88	A8
9	F9	C9	D9	E9	B9	99	89	A9
18	79	49	59	69	B0	90	80	A0
28	7A	4A	5A	E0	BA	9A	8A	AA
38	7B	4B	5B	6B	BB	9B	8B	AB
48	7C	4C	5C	6C	BC	9C	8C	AC
58	7D	4D	5D	6D	BD	9D	8D	AD
68	7E	4E	5E	6E	BE	9E	8E	AE
78	7F	4F	5F	6F	BF	9F	8F	AF
19	31	01	11	21	71	51	41	E1
29	32	02	12	22	72	52	42	62
39	33	03	13	23	73	53	43	63
49	34	04	14	24	74	54	44	64
59	35	05	15	25	75	55	45	65
69	36	06	16	26	76	56	46	66
79	37	07	17	27	77	57	47	67
89	38	08	18	28	78	58	48	68
189	39	09	19	29	30	10	00	20
289	3A	0A	1A	2A	FA	DA	CA	EA
389	3B	0B	1B	2B	FB	DB	CB	EB
489	3C	0C	1C	2C	FC	DC	CC	EC
589	3D	0D	1D	2D	FD	DD	CD	ED
689	3E	0E	1E	2E	FE	DE	CE	EE
789	3F	0F	1F	2F	FF	DF	CF	EF

Bl = Blank
T = Twelve
E = Eleven
O = Zero

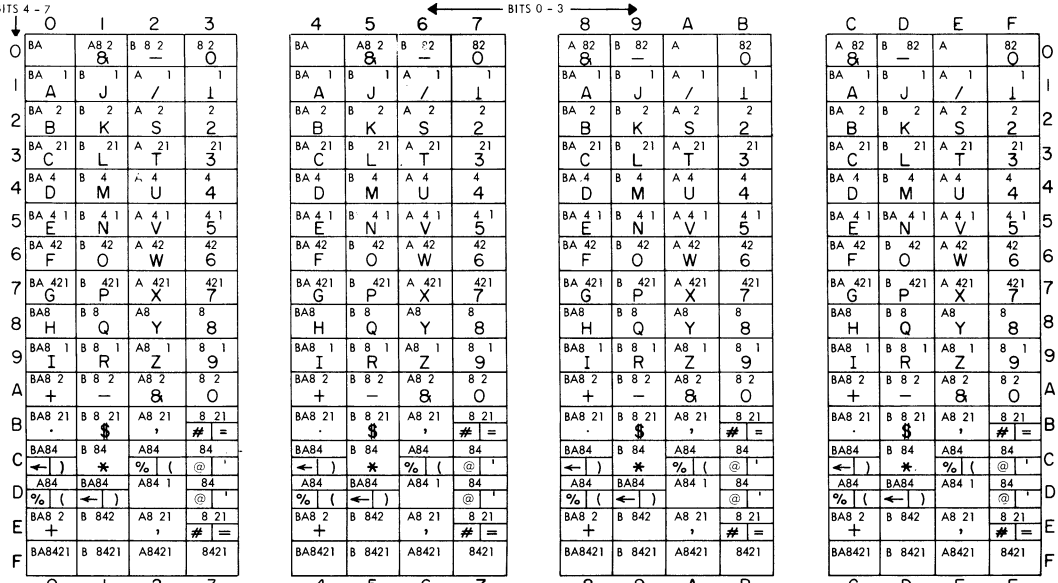
American Standard Code for Information Interchange (ASCII)
Extended to Eight Bits

Bit Positions → 76 / X5 / 4321	00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
0000	NULL	DC_0			b blank	0					@	P				P
0001	SOM	DC_1			!	1					A	Q			a	q
0010	EOA	DC_2			"	2					B	R			b	r
0011	EOM	DC_3			#	3					C	S			c	s
0100	EOT	DC_4 STOP			$	4					D	T			d	t
0101	WRU	ERR			%	5					E	U			e	u
0110	RU	SYNC			&	6					F	V			f	v
0111	BELL	LEM			'	7					G	W			g	w
1000	BKSP	S_0			(	8					H	X			h	x
1001	HT	S_1			)	9					I	Y			i	y
1010	LF	S_2			*	:					J	Z			j	z
1011	VT	S_3			+	;					K	[			k	
1100	FF	S_4			,	<					L	\			l	
1101	CR	S_5			-	=					M	]			m	
1110	SO	S_6			.	>					N	↑			n	ESC
1111	SI	S_7			/	?					O	←			o	DEL

ZONE AND 8-9 PUNCHES	DIGIT PUNCHES 1-7																								
		1403	1443	1	1403	1443	2	1403	1443	3	1403	1443	4	1403	1443	5	1403	1443	6	1403	1443	7	1403	1443
12-9	C9	I	I	01			02			03			04			05			06			07		
12-8-9	08			09			0A			0B			0C			0D			0E			0F		
11-9	D9	R	R	11			12			13			14			15			16			17		
11-8-9	18			18			1A			1B			1C			1D			1E			1F		
0-9	E9	Z	Z	21			22			23			24			25			26			27		
0-8-9	28			29			2A			2B			2C			2D			2E			2F		
9	F9	9	9	31			32			33			34			35			36			37		
8-9	38			39			3A			3B			3C			3D			3E			3F		
12-0-9	89			41			42			43			44			45			46			47		
12-8	C8	H	H	49			4A			4B			4C	¤	←	4D		(	4E		+	4F		±
12-11-9	99			51			52			53			54			55			56			57		
11-8	D8	Q	Q	59			5A			5B	$	$	5C	*	*	5D		)	5E		;	5F		¢
11-0-9	A9			E1			62			63			64			65			66			67		
0-8	E8	Y	Y	69			E0			6B	,	,	6C	%	%	6D		∨	6E		-	6F		±
12-11-0-9	B9			71			72	‡	‡	73			74			75			76			77		
8	F8	8	8	79			7A	∓	:	7B	#	#	7C	@	@	7D		·	7E		=	7F		✓
12-0	C0	&	>	81			82			83			84			85			86			87		
12-0-8	88			80			8A			8B			8C			8D			8E			8F		
12-11	6A			91			92			93			94			95			96			97		
12-11-8	98	-	<	90			9A			9B			9C			9D			9E			9F		
11-0	D0			A1			A2			A3			A4			A5			A6			A7		
11-0-8	A8			A0			AA			AB			AC			AD			AE			AF		
12-11-0	70			B1			B2			B3			B4			B5			B6			B7		
12-11-0-8	B8			B0			BA			BB			BC			BD			BE			BF		
12	50	&	&	C1	A	A	C2	B	B	C3	C	C	C4	D	D	C5	E	E	C6	F	F	C7	G	G
12-0-8-9	48			00			CA			CB			CC			CD			CE			CF		
11	60	-	-	D1	J	J	D2	K	K	D3	L	L	D4	M	M	D5	N	N	D6	0	0	D7	P	P
12-11-8-9	58			10			DA			DB			DC			DD			DE			DF		
0	F0	0	0	61	/	/	E2	S	S	E3	T	T	E4			E5	V	V	E6	W	W	E7	X	X
11-0-8-9	68			20			EA			EB			EC			ED			EE			EF		
NONE	40			F1	1	1	F2	2	2	F3	3	3	F4	4	4	F5	5	5	F6	6	6	F7	7	7
12-11-0-8-9	78			30			FA			FB			FC			FD			FE			FF		

* 1403 Graphics are for Type "A" chain

** 1443 Graphics are, as shown, for 1443N1 with 63 Character SMS Bar.


BITS 4 - 7
BITS 0 - 3
0 1 2 3
4 5 6 7
8 9 A B
C D E F

Character in Order of Sequence on the Chain (Standard)	BCD Code in PCG					
	B	A	8	4	2	1
1						1
2					2	
3					2	1
4				4		
5				4		1
6				4	2	
7				4	2	1
8			8			
9			8			1
0			8		2	
#			8		2	1
@			8	4		
/		A				1
S		A			2	
T		A			2	1
U		A		4		
V		A		4		1
W		A		4	2	
X		A		4	2	1
Y		A	8			
Z		A	8			1
&		A	8		2	
,		A	8		2	1
%		A	8	4		
J	B					1
K	B				2	
L	B				2	1
M	B			4		
N	B			4		1
O	B			4	2	
P	B			4	2	1
Q	B		8			
R	B		8			1
—	B		8		2	
$	B		8		2	1
*	B		8	4		
A	B	A				1
B	B	A			2	
C	B	A			2	1
D	B	A		4		
E	B	A		4		1
F	B	A		4	2	
G	B	A		4	2	1
H	B	A	8			
I	B	A	8			1
+	B	A	8		2	
.	B	A	8		2	1
←	B	A	8	4		

Collating	Graphics		8 Bit Code								BCD					
Sequence	8 Bit	BCD	0	1	2	3	4	5	6	7	B	A	8	4	2	1
00	blank	blank	0	1	0	0	0	0	0	0	0	0	0	0	0	0
01	.	.	0	1	0	0	1	0	1	1	1	1	1	0	1	1
02	←	X)	0	1	0	0	1	1	0	0	1	1	1	1	0	0
03	(	⌐	0	1	0	0	1	1	0	1	1	1	1	1	0	1
04	+	<	0	1	0	0	1	1	1	0	1	1	1	1	1	0
05	GM	GM	0	1	0	0	1	1	1	1	1	1	1	1	1	1
06	&	& +	0	1	0	1	0	0	0	0	1	1	0	0	0	0
07	$	$	0	1	0	1	1	0	1	1	1	0	1	0	1	1
08	*	*	0	1	0	1	1	1	0	0	1	0	1	1	0	0
09	)	¬	0	1	0	1	1	1	0	1	1	0	1	1	0	1
10	;	;	0	1	0	1	1	1	1	0	1	0	1	1	1	0
11	MC	MC	0	1	0	1	1	1	1	1	1	0	1	1	1	1
12	-	-	0	1	1	0	0	0	0	0	1	0	0	0	0	0
13	/	/	0	1	1	0	0	0	0	1	0	1	0	0	0	1
14	,	,	0	1	1	0	1	0	1	1	0	1	1	0	1	1
15	%	% (	0	1	1	0	1	1	0	0	0	1	1	1	0	0
16	WS	WS	0	1	1	0	1	1	0	1	0	1	1	1	0	1
17	↑	\	0	1	1	0	1	1	1	0	0	1	1	1	1	0
18	SM	SM	0	1	1	0	1	1	1	1	0	1	1	1	1	1
19	ъ	ъ	0	1	1	1	1	0	1	0	0	1	0	0	0	0
20	"	"=	0	1	1	1	1	0	1	1	0	0	1	0	1	1
21	@	@ '	0	1	1	1	1	1	0	0	0	0	1	1	0	0
22	▽	:	0	1	1	1	1	1	0	1	0	0	1	1	0	1
23	=	>	0	1	1	1	1	1	1	0	0	0	1	1	1	0
24	TM	TM	0	0	0	1	0	0	1	1	0	0	1	1	1	1
25	±	±	1	1	0	0	0	0	0	0	1	1	1	0	1	0
26	A	A	1	1	0	0	0	0	0	1	1	1	0	0	0	1
27	B	B	1	1	0	0	0	0	1	0	1	1	0	0	1	0
28	C	C	1	1	0	0	0	0	1	1	1	1	0	0	1	1
29	D	D	1	1	0	0	0	1	0	0	1	1	0	1	0	0
30	E	E	1	1	0	0	0	1	0	1	1	1	0	1	0	1
31	F	F	1	1	0	0	0	1	1	0	1	1	0	1	1	0
32	G	G	1	1	0	0	0	1	1	1	1	1	0	1	1	1

Collating Sequence	Graphics		8 Bit Code								BCD					
	8Bit	BCD	0	1	2	3	4	5	6	7	B	A	8	4	2	1
33	H	H	1	1	0	0	1	0	0	0	1	1	1	0	0	0
34	I	I	1	1	0	0	1	0	0	1	1	1	1	0	0	1
35	$\bar{o}$	$\bar{o}$	1	1	0	1	0	0	0	0	1	0	1	0	1	0
36	J	J	1	1	0	1	0	0	0	1	1	0	0	0	0	1
37	K	K	1	1	0	1	0	0	1	0	1	0	0	0	1	0
38	L	L	1	1	0	1	0	0	1	1	1	0	0	0	1	1
39	M	M	1	1	0	1	0	1	0	0	1	0	0	1	0	0
40	N	N	1	1	0	1	0	1	0	1	1	0	0	1	0	1
41	O	O	1	1	0	1	0	1	1	0	1	0	0	1	1	0
42	P	P	1	1	0	1	0	1	1	1	1	0	0	1	1	1
43	Q	Q	1	1	0	1	1	0	0	0	1	0	1	0	0	0
44	R	R	1	1	0	1	1	0	0	1	1	0	1	0	0	1
45	RM	RM	1	1	1	0	0	0	0	0	0	1	1	0	1	0
46	S	S	1	1	1	0	0	0	1	0	0	1	0	0	1	0
47	T	T	1	1	1	0	0	0	1	1	0	1	0	0	1	1
48	U	U	1	1	1	0	0	1	0	0	0	1	0	1	0	0
49	V	V	1	1	1	0	0	1	0	1	0	1	0	1	0	1
50	W	W	1	1	1	0	0	1	1	0	0	1	0	1	1	0
51	X	X	1	1	1	0	0	1	1	1	0	1	0	1	1	1
52	Y	Y	1	1	1	0	1	0	0	0	0	1	1	0	0	0
53	Z	Z	1	1	1	0	1	0	0	1	0	1	1	0	0	1
54	0	0	1	1	1	1	0	0	0	0	0	0	1	0	1	0
55	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	1
56	2	2	1	1	1	1	0	0	1	0	0	0	0	0	1	0
57	3	3	1	1	1	1	0	0	1	1	0	0	0	0	1	1
58	4	4	1	1	1	1	0	1	0	0	0	0	0	1	0	0
59	5	5	1	1	1	1	0	1	0	1	0	0	0	1	0	1
60	6	6	1	1	1	1	0	1	1	0	0	0	0	1	1	0
61	7	7	1	1	1	1	0	1	1	1	0	0	0	1	1	1
62	8	8	1	1	1	1	1	0	0	0	0	0	1	0	0	0
63	9	9	1	1	1	1	1	0	0	1	0	0	1	0	0	1

*BCD code for blank is:
C bit for odd parity
C and A bits for even parity

HEXADECIMAL AND DECIMAL CONVERSION

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1	

HEXADECIMAL ADDITION

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

HEXADECIMAL MULTIPLICATION

1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

POWERS OF 16		POWERS OF 2	
16^n	n	2^n	n
1	0	512	9
16	1	1 024	10
256	2	2 048	11
4 096	3	4 096	12
65 536	4	8 192	13
1 048 576	5	16 384	14
16 777 216	6	32 768	15
268 435 456	7	65 536	16
4 294 967 296	8	131 072	17
68 719 476 736	9	262 144	18
1 099 511 627 776	10	524 288	19
17 592 186 044 416	11	1 048 576	20
281 474 976 710 656	12	2 097 152	21
4 503 599 627 370 496	13	4 194 304	22
72 057 594 037 927 936	14	8 388 608	23
1 152 921 504 606 846 976	15	16 777 216	24

All diagnostic programs are listed in CEM #2 of System/360 Diagnostics Section, Group 15 CEMs. The Diagnostic CEMs are on microfiche card CJ221.

The meaning of the prefix of the diagnostic ID (identification) is:

0 - Special system (non-System/360)
1 - Not used
2 - Used by Model 20
3 - Used by Model 30
4 - Used by Models 40/44
5 - Used by Model 50
6 - Used by Models 65/67
7 - Used by Model 75
8 - Used by Model 85
9 - Used by Models 91/95
A - On line test
B - Not used
C - Used by Model 25
D - Special system (FAA 9020)
E - Used by some systems but not by all
F - Applicable to all systems

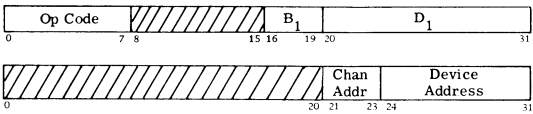
Also refer to:
Reference Manual, Diagnostic Monitor, Form 229-2125
Reference Manual, Diagnostic Section, Form 229-2127
and to other system handbooks.

PERMANENT STORAGE ASSIGNMENT

ADDRESS			LENGTH	PURPOSE
DEC	HEX	BINARY		
0	0	0000 0000	doubleword	Initial program loading PSW
8	8	0000 1000	doubleword	Initial program loading CCW1
16	10	0001 0000	doubleword	Initial program loading CCW2
24	18	0001 1000	doubleword	External old PSW
32	20	0010 0000	doubleword	Supervisor call old PSW
40	28	0010 1000	doubleword	Program old PSW
48	30	0011 0000	doubleword	Machine-check old PSW
56	38	0011 1000	doubleword	Input/output old PSW
64	40	0100 0000	doubleword	Channel status word
72	48	0100 1000	word	Channel address word
76	4C	0100 1100	word	Unused
80	50	0101 0000	word	Timer
84	54	0101 0100	word	Unused
88	58	0101 1000	doubleword	External new PSW
96	60	0110 0000	doubleword	Supervisor call new PSW
104	68	0110 1000	doubleword	Program new PSW
112	70	0111 0000	doubleword	Machine-check new PSW
120	78	0111 1000	doubleword	Input/output new PSW
128	80	1000 0000	(1)	Diagnostic scan-out area

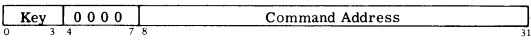
(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

SI Format

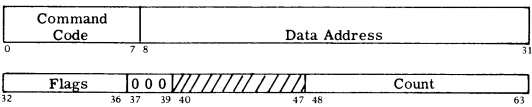


D1(B1)
S1
} HIO, SIO, TCH, TIO

CHANNEL ADDRESS WORD



CHANNEL COMMAND WORD



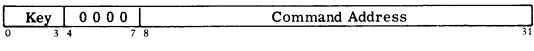
Command Code assignments are listed in the following table. The symbol **X** indicates that the bit position is ignored; **M** identifies a modifier bit.

CODE	COMMAND
MMMM 0 1 0 0	Sense
XXX X 1 0 0 0	Transfer in channel
MMMM 1 1 0 0	Read backward
MMMM MM0 1	Write
MMMM MM1 0	Read
MMMM MM1 1	Control

Bits 0-7 specify the command code.
Bits 8-31 specify the location of a byte in main storage.
Bits 32-36 are flag bits; refer to OPERATION CODE tables for flag bit assignments.
- Bit 32 causes the address portion of the next CCW to be used.
- Bit 33 causes the command code and data address in the next CCW to be used.
- Bit 34 causes a possible incorrect length indication to be suppressed.
- Bit 35 suppresses the transfer of information to main storage.
- Bit 36 causes an interruption as Program Control Interrupt

Bits 37-39 must contain zeros.
Bits 40-47 are ignored.
Bits 48-63 specify the number of bytes in the operation.

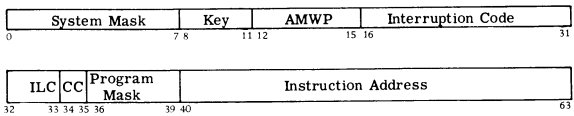
CHANNEL STATUS WORD



32 Attention
33 Status modifier
34 Control unit end
35 Busy
36 Channel end
37 Device end
38 Unit check
39 Unit exception
40 Program-controlled interruption
41 Incorrect length
42 Program check
43 Protection check
44 Channel data check
45 Channel control check
46 Interface control check
47 Chaining check

Count: Bits 48-63 form the residual count for the last CCW used.

PROGRAM STATUS WORD



0-7 System mask
0 Multiplexer channel mask
1 Selector channel 1 mask
2 Selector channel 2 mask
3 Selector channel 3 mask
4 Selector channel 4 mask
5 Selector channel 5 mask
6 Selector channel 6 mask
7 External mask
8-11 Protection key
12 ASCII mode (A)
13 Machine check mask (M)
14 Wait state (W)
15 Problem state (P)
16-31 Interruption code
32-33 Instruction Length code (ILC)
34-35 Condition code (CC)
36-39 Program mask
36 Fixed-point overflow mask
37 Decimal overflow mask
38 Exponent underflow mask
39 Significance mask
40-63 Instruction address

Command for CCW		Count	Multiple Track (M-T) Off 8-Bit Code 0123 4567	Hex Dec	M-T On † Hex Dec
Control	No Op	X	0000 0011	03 03	
	Seek	6	0000 0111	07 07	
	Seek Cylinder	6	0000 1011	0B 11	
	Seek Head	6	0001 1011	1B 27	
	Set File Mask	1	0001 1111	1F 31	
	Space Count	X	0000 1111	0F 15	
	Transfer in Channel	X	XXXX 1000	X8	
	Recalibrate (2311 only)		0001 0011	13 19	
	Restore (2321 only)	X	0001 0111	17 23	
Sense	Sense I/O	4	0000 0100	04 04	
Switching	Release Device	X	1001 0100	94 148	
	Reserve Device	X	1011 0100	B4 180	
Search †	Home Address EQ	4 (usually)	0011 1001	39 57	B9 185
	Identifier EQ	5 (usually)	0011 0001	31 49	B1 177
	Identifier HI	5 (usually)	0101 0001	51 81	D1 209
	Identifier EQ or HI	5 (usually)	0111 0001	71 113	F1 241
	Key EQ	1 to 255	0010 1001	29 41	A9 169
	Key HI	1 to 255	0100 1001	49 73	C9 201
	Key EQ or HI	1 to 255	0110 1001	69 105	E9 233
	Key & Data EQ*	Note 1	0010 1101	2D 45	AD 173
	Key & Data HI*		0100 1101	4D 77	CD 205
	Key & Data EQ or HI*		0110 1101	6D 109	ED 237
	Continue Scan EQ*		0010 0101	25 37	
	Continue Scan HI*		0100 0101	45 69	
	Continue Scan EQ or HI*		0110 0101	65 101	
	Continue Scan No Compare*		0101 0101	55 85	
	Continue Scan Set Compare*		0111 0101	75 117	
Read †	Home Address	5	0001 1010	1A 26	9A 154
	Count	8	0001 0010	12 18	92 146
	Record R0	Number	0001 0110	16 22	96 150
	Data	of bytes	0000 0110	06 06	86 134
	Key & Data	trans-	0000 1110	0E 14	8E 142
	Count, Key & Data	ferred	0001 1110	1E 30	9E 158
	Initial Program Load (IPL)		0000 0010	02 02	
Write	Home Address	5 (usually)	0001 1001	19 25	
	Record R0	8+KL+DL of R0	0001 0101	15 21	
	Count, Key & Data	8+KL+DL	0001 1101	1D 29	
	Special Count, Key & Data*	8+KL+DL	0000 0001	01 01	
	Data	DL	0000 0101	05 05	
	Key & Data	KL & DL	0000 1101	0D 13	

* Special Feature Note 1. Includes mask bytes in search argument.
† M-T On = M-T Off except, during Search and Read bit 0 = 1 in M-T On.
X = not significant; KL = Key Length DL = Data Length; EQ = Equal; HI = High

Device	Command for CCW	8-Bit Code 0	1	2	3	4	5	6	7	Hex	Dec
1052	Read Inquiry BCD	0	0	0	0	1	0	1	0	0A	10
	Read Reader 2 BCD	0	0	0	0	0	0	1	0	02	02
	Write BCD, Auto Carriage Return	0	0	0	0	1	0	0	1	09	09
	Write BCD, No Auto Carriage Return	0	0	0	0	0	0	0	1	01	01
	No Op	0	0	0	0	0	0	1	1	03	03
	Sense	0	0	0	0	0	1	0	0	04	04
	Alarm	0	0	0	0	1	0	1	1	0B	11
2540	Read, Feed, Select Stacker SS — Type AA	S	S	D	0	0	0	1	0		
	Read — Type AB	1	1	D	0	0	0	1	0		
	Read, Feed (1400 compatability mode only)	1	1	D	1	0	0	1	0		
	Feed, Select Stacker SS — Type BA	S	S	1	0	0	0	1	1		
	PFR Punch, Feed, Select Stacker SS — Type BA	S	S	D	0	1	0	0	1		
	Punch, Feed, Select Stacker SS — Type BB	S	S	D	0	0	0	0	1		
1442 N1	Read	M	M	M	0	0	0	1	0		
	Write	M	M	M	0	0	0	0	1		
	Control	M	M	0	0	0	0	1	1		
	No Op	0	0	0	0	0	0	1	1		
	Sense	0	0	M	M	0	1	0	0		
1403 or 1443	Write, No Space	0	0	0	0	0	0	0	1	01	01
	Write, Space 1 After Print	0	0	0	0	1	0	0	1	09	09
	Write, Space 2 After Print	0	0	0	1	0	0	0	1	11	17
	Write, Space 3 After Print	0	0	0	1	1	0	0	1	19	25
	Write, Skip To Channel N After Print	1	C	H	A	N	0	0	1		
	Diagnostic Read (1403)	0	0	0	0	0	0	1	0	02	02
	Diagnostic Read (1443)	0	0	0	0	0	1	1	0	06	06
	Test I/O	0	0	0	0	0	0	0	0	00	00
	Sense	0	0	0	0	0	1	0	0	04	04
Carriage Control	Space 1 Line Immediately	0	0	0	0	1	0	1	1	0B	11
	Space 2 Line Immediately	0	0	0	1	0	0	1	1	13	19
	Space 3 Line Immediately	0	0	0	1	1	0	1	1	1B	27
	Skip To Channel N Immediately	1	C	H	A	N	0	1	1		
	No Op	0	0	0	0	0	0	1	1	03	03
2400 Tape*	Transfer in Channel	0	0	0	0	1	0	0	0	08	08
	Sense	0	0	0	0	0	1	0	0	04	04
	Read Backward**	0	0	0	0	1	1	0	0	0C	12
	Write	0	0	0	0	0	0	0	1	01	01
	Read	0	0	0	0	0	0	1	0	02	02
	Control	0	0	C	C	C	1	1	1		
	Mode Set	D	D	M	M	M	0	1	1		

SS	Stacker
00	R1
01	R2
10	RP3

D	Data Mode
0	EBCDIC
1	Column Binary

X = 0 means EBCDIC mode
X = 1 means Column Binary Mode

C	H	A	N	Channel
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12

* 9 track op. forces 800 BPI and odd parity; also, it overrides 7 track but does not reset 7 track. Load/Sys Reset forces 7 track to 800 BPI, odd parity, data converter on, translator off.

C	C	C	Control Codes	Hex	Dec
0	0	0	REW	7	7
0	0	1	RUN	0F	15
0	1	0	ERG	17	23
0	1	1	WTM	1F	31
1	0	0	BSR	27	39
1	0	1	BSF	2F	47
1	1	0	FSR	37	55
1	1	1	FSF	3F	63

D	D	7 Track Density
0	0	200
0	1	556
1	0	800
1	1	800

**Overrides Data Converter On

M M M (Mode Modifiers)

	Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request TIE (Track in Error)
0 0 0 No Op								
0 0 1 Not Used								
0 1 0 Reset Condition	X	X		X			X	
0 1 1 Misc. track only								X
1 0 0	X		X		X		X	
1 0 1	X		X		X	X		
1 1 0 Reset Condition	X	X			X			X
1 1 1	X	X			X	X		

Interruption	Interruption Code (PSW Bits 16-31)	PSW Mask Bit	ILC	How Instruction Execution Is Finished
Machine Check	cccccccc cccccccc	13	u	Terminated
Program				
Operation	00000000 00000001	-	1, 2, 3	Suppressed
Privileged operation	00000000 00000010	-	1, 2	Suppressed
Execute	00000000 00000011	-	2	Suppressed
Protection	00000000 00000100	-	0, 2, 3	Suppressed/Term
Addressing	00000000 00000101	-	0, 1, 2, 3	Suppressed/Term
Specification	00000000 00000110	-	1, 2, 3	Suppressed
Data	00000000 00000111	-	2, 3	Suppressed Term
Fixed-point overflow	00000000 00001000	36	1, 2	Completed
Fixed-point divide	00000000 00001001	-	1, 2	Suppressed/Comp
Decimal overflow	00000000 00001010	37	3	Completed
Decimal divide	00000000 00001011	-	3	Suppressed
Exponent overflow	00000000 00001100	-	1, 2	Completed
Exponent underflow	00000000 00001101	38	1, 2	Completed
Significance	00000000 00001110	39	1, 2	Completed
Floating-point divide	00000000 00001111	-	1, 2	Suppressed
Supervisor Call	00000000 rrrrrrrr	-	1	Completed

External				
External signal 7	00000000 nnnnnnnl	7	u	Completed
External signal 6	00000000 nnnnnnln	7	u	Completed
External signal 5	00000000 nnnnnlnn	7	u	Completed
External signal 4	00000000 nnnnlnnn	7	u	Completed
External signal 3	00000000 nnnlnnnn	7	u	Completed
External signal 2	00000000 nnlnnnnn	7	u	Completed
INTERRUPT pushbutton	00000000 nlnnnnnn	7	u	Completed
Timer	00000000 lnnnnnnn	7	u	Completed
I/O				
Multiplexer channel	00000000 aaaaaaaa	0	u	Completed
Selector channel 1	00000001 aaaaaaaa	1	u	Completed
Selector channel 2	00000010 aaaaaaaa	2	u	Completed
Selector channel 3	00000011 aaaaaaaa	3	u	Completed
Selector channel 4	00000100 aaaaaaaa	4	u	Completed
Selector channel 5	00000101 aaaaaaaa	5	u	Completed
Selector channel 6	00000110 aaaaaaaa	6	u	Completed

Notes: u: Unpredictable
r: I-field of Supervisor Call instruction
a: I/O device address
n: Other external-interruption conditions.

CIRCUIT DATA

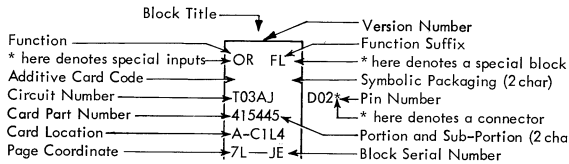
Definitions of ALD Page Number Prefixes

I.	Adders	
	1. Addressing Adder	AA-AB
	2. IC Incrementer	AC-AD
	3. Exponent Adder	AE-AF
	4. Main Adder	AM-AQ
	5. Serial Adder	AS
	6. VFL and DEC Adder	AV-AW
II.	Decoders	
	1. Op Decoders	DN
	2. FLP and Gen. Decoder	DP
	3. Addressing and Pre FTH	DA
	4. Trap Decode	DB
	5. Reg Decode	DG
	6. ROM Decode	DR-DS
III.	Counters	
	1. Instruction Ctrs	CA-CB
	2. Local Store Address Ctr	CC-CD
	3. Misc. Ctr	CE-CZ
IV.	Busing (Excluding Memory Bus)	BA-BZ
V.	Registers	
	1. A Reg	RA
	2. B Reg (BOP REG, Mod 70)	RB
	3. D Reg	RD
	4. E Reg (PSW for Mod 70)	RE
	5. F Reg (I/O Reg, Mod 70)	RF
	6. G Reg (Gen Purpose, Mod 70)	RG
	7. H Reg	RH
	8. J Reg	RJ
	9. K Reg	RK
	10. L Reg	RL
	11. M Reg	RM
	12. N Reg (Op Code Reg, Mod 70)	RN
	13. P Reg (FLT Pt Reg, Mod 70)	RP
	14. Q Reg (FLT Pt Reg, Mod 70)	RQ
	15. R Reg (Reg Bus Latch, Mod 70)	RR
	16. S Reg (Shift Ctr and Exp in, Mod 70)	RS
	17. T Reg	RT
	18. U Reg	RU
	19. V Reg	RV
	20. W Reg	RW
	21. X Reg	RX
	22. VFL and Decoder Reg, Mod 70	RY
	23. Direct Data Reg	RZ

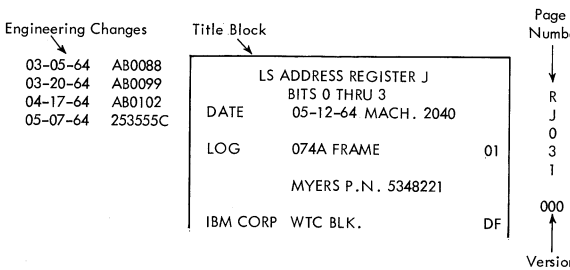
VI.	Main Storage Registers and Controls in CPU (Includes SDR Registers, Storage Buses, SAR, SBI "OR", M and N Registers in Mod 30)	MA-MC
VII.	Controls	
	1. Advance or Seq Cntls	KA
	2. Branch and IC Cntls	KB
	3. Clock Cntls	KC
	4. I Exec (Mod 70) I Fetch and Exec (Mod 60)	KD
	5. Chan Cntls	KE
	6. Fix Seq Cntls	KF
	7. Gen Reg Cntls	KG
	8. FLT Cntls	KH
	9. ROS Cntls	KK
	10. Local Store Cntls	KL
	11. Priority and Interrupt Cntls	KM
	12. I/O Instr Cntls	KN
	13. VFL Cntls	KP
	14. VFL Cntls	KQ
	15. Check Triggers	KR
	16. Status Triggers	KS
	17. VFL Cntls and Decimal Cntls	KY
	18. Any Misc. Cntls such as FP	KT-KU
	19. Fixed Pt, Storage Protect, Real Time clk, Status Cntls	KW-KZ
VIII.	Consoles	PA-PE, PJ-PZ
	1052 Console Adapter	PF,PG,PH
IX.	Local Store	LS-LT
X.	TROS	EA-EC
XI.	CROS	ED-EF
XII.	Spec Features	XA-XZ
XIII.	Hardware Oriented Pages	ZA-ZZ
XIV.	I/O Channels	
	Multiplex Channel	FA-FZ
	Selector Channel No. 1	GA-GZ
	Selector Channel No. 2	HA-HZ
	Direct Data	JA-JZ
XV.	ROS Flow charts	QA-QZ
XVI.	Power Supplies	YA-YZ

Engineering ALD

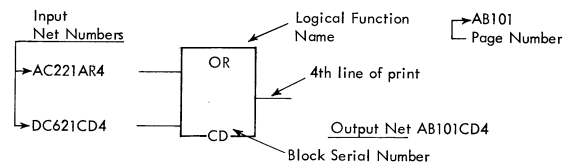
Eng ALD Logic Block



ALD Title Block, Page Number and Version, and Engineering Changes



Net Numbers



Connector Location Designations

SLT Logic Connector:

01	A-	D3	B2	D09
Frame	Gate	Board	Socket	Pin

ASLT Logic Connector:

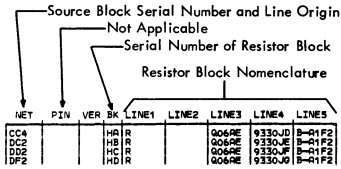
BL4	B-	A1	E6	D02
Connector Source	Gate	Board	Socket	Pin

Resistor Listing:

CC4	HA	R	Q06AE	9330JD	B-A1F2
Source Block	Serial Number of Resistor Block	Function	Circuit Number	Card Part Number and Portion Number	Card Location

Engineering ALD (Continued)

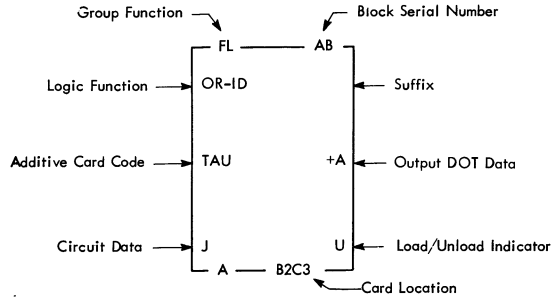
ALD Resistor Chart



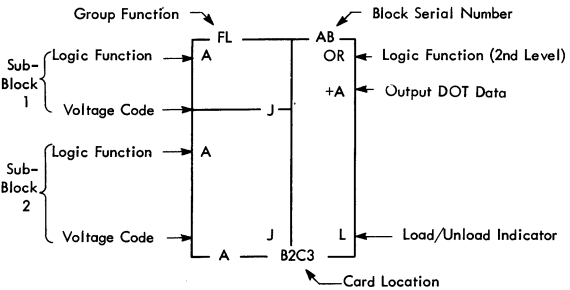
FE ALD

FE ALD Logic Block

Single Block

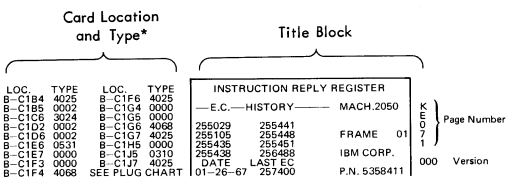


Butted Block



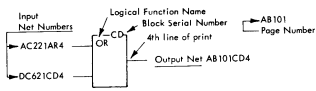
FE ALD (Continued)

Title Block, Page Number and Version



*Check Socket Listing for part number

Net Numbers



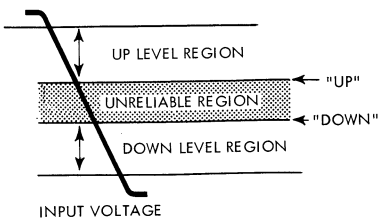
Connector Location Designations

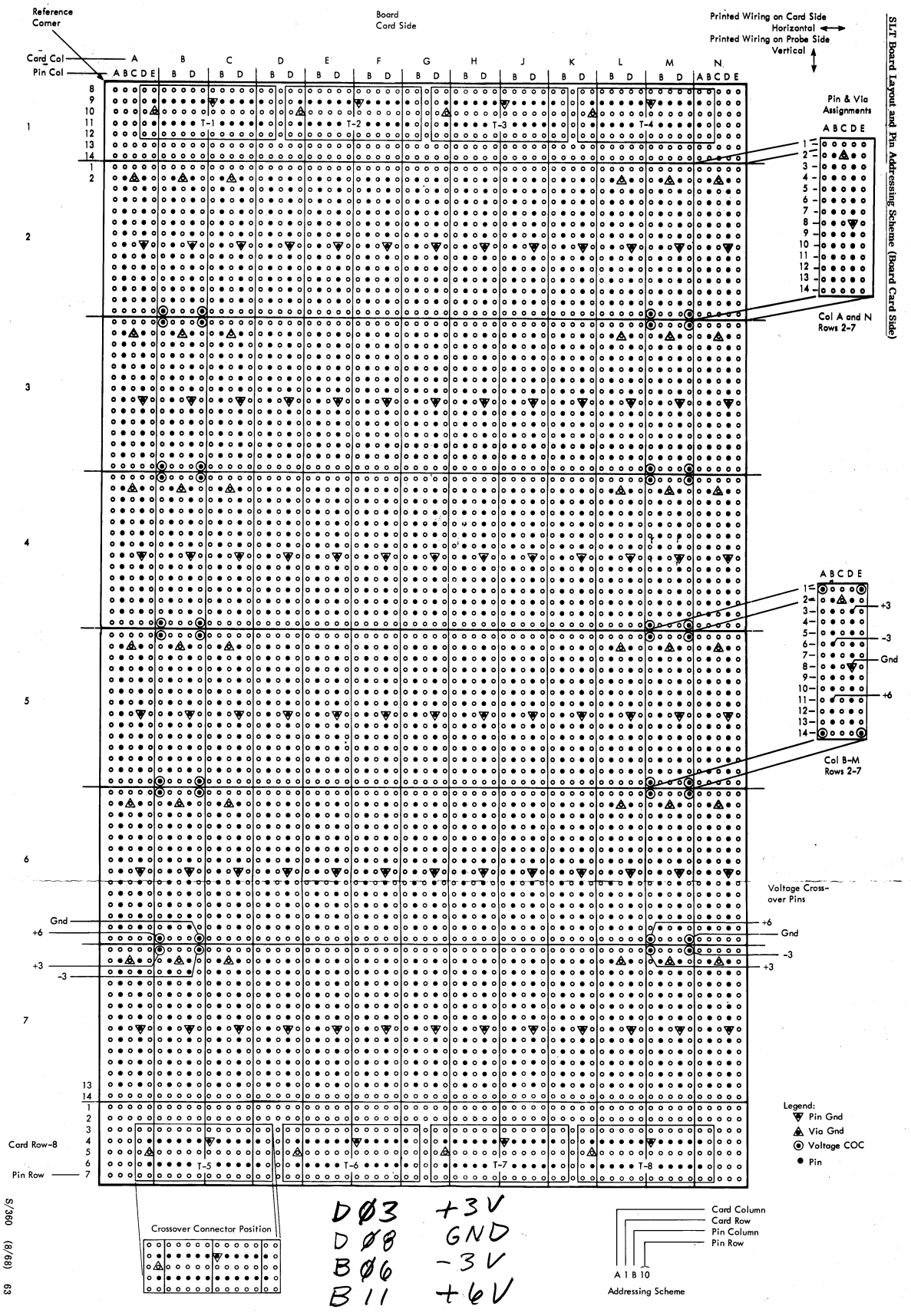
Logic Connector or Resistor:

01	A–	D3	B2	D09
Frame	Gate	Board	Socket	Pin

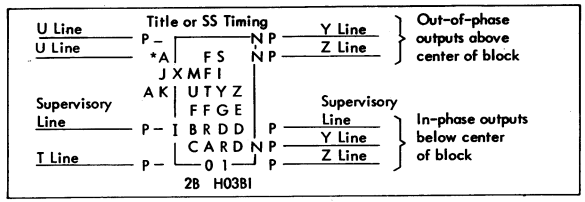
FE ALD Voltage Code

Code	Up	Down
B	+2.5	+1.5
C	+2.5	+1.0
D	+1.9	+1.0
E	+2.0	+ .6
F	+4.0	+ .3
G	+2.5	+ .3
H	+2.0	+ .3
J	+1.5	+ .3
L	+ .6	+ .3
M	unassigned	
P	unassigned	
Q	unassigned	
R	unassigned	
S	unassigned	
T	+ .3	– .3
U	unassigned	
V	unassigned	
W	unassigned	
Y	unassigned	
Z	unassigned	




Reference Corner
Board Card Side
Printed Wiring on Card Side Horizontal
Printed Wiring on Probe Side Vertical
Card Col
Pin Col
A B C D E
B D
T-1
T-2
T-3
T-4
T-5
T-6
T-7
T-8
Pin & Via Assignments
Col A and N Rows 2-7
Col B-M Rows 2-7
+3
-3
Gnd
+6
Voltage Cross-over Pins
Card Row-8
Pin Row
Crossover Connector Position
D Ø3 +3V
D Ø8 GND
B Ø6 -3V
B 11 +6V
Legend:
Pin Gnd
Via Gnd
Voltage COC
Pin
Card Column
Card Row
Pin Column
Pin Row
A 1 B 10
Addressing Scheme

SMS ALD Logic Block



FS - Functional symbol (up to four characters -A, -TO, SS, ---)
MFI - Machine feature index or special note (up to four characters)
UT - Line type in
YZ - Line type out
FF - Frame (01 - 99)
G - Sliding gate (A, B, C, D) or module (A, B, C, ---)
E - Engineering change level tag (A, B, C, ---)
B - Chassis (1 - 6) or swinging gate (1 - 8)
R - Chassis Row (A - K) or swinging gate column (A - F)
DD - Chassis column (01 - 28) or swinging gate row (01 - 26)
P - Card socket pin (single card: A-R; double, Stan-Pac, or twin: A-8)
*A - Edge Connector, Test-Point given in Note A
JX - Shield lead connected to pin J (X = twisted pair; * = coaxial cable)
AK - Pin A backpanel wired to pin K
CARD - Card code
2B - Page coordinates
H03BI - For engineering use; block identification (circuit type)
01 - For engineering use; block configuration (01, 02, 03, ---)
N - When used means normal (not supervisory) output, load in this block.
I - One of six symbols:
- 3 - Third level input, load in this block
- ◊ - Third level input, load elsewhere
- S - Split level input, load in this block
- 2 - Split level input, load elsewhere
- C - Cascode level input, load in this block
- H - Cascode level input, load elsewhere

SMS Line Levels

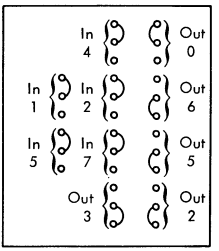
Line Type	Ideal Swing (volts)	Down Levels (volts)		Up Levels (volts)		Application
		Low	High	Low	High	
B	0 to + 6	+ 0.1	+ 0.3	+2.7	+6.8	DDTL, Uncompensated
B	0 to + 6	+ 0.1	+ 0.3	+5.6	+6.8	DDTL, Compensated
B	0 to + 6	- 0.8	+ 0.8	+3.2	+6.8	DDTL, DE Chain
C	0 to 15 ma	- 4.1	- 0.3	+0.6	+3.1	Std Interface DL, DT
D	-2.5 to +2.5	- 5.0	- 0.7	+0.7	+5.0	DEFL
E	-6 to +6	- 25.0	- 3.0	+3.0	+25.0	EIA Std Data Sets
E_S	+0.0 to -12.6	- 3.09	-12.6	+0.2	-0.0	SMAL Logic
N	± from 0 ref	- 3.0	- 0.4	+0.4	+1.2	Alloy Current Sw
N	± from 0 ref	- 0.9	- 0.4	+0.4	+0.6	Diffused Current Sw
P	± from -6 ref	- 7.2	- 6.4	-5.6	-3.0	Alloy Current Sw
P	± from -6 ref	- 6.6	- 6.4	-5.6	-5.2	Diffused Current Sw
Q	0 to 40 ma	- 3.8	- 0.5*	+0.6	+2.4	DL and DT
R	0 to +12	- 0.4	+ 0.2	+5.6	+12.5	CTRL
S	-12 to 0	-12.5	- 5.6	-0.2	+0.4	CTRL
S	-12 to 0	-12.5	- 6.9	-0.5	0.0	SDTRL
S'	-6 to 0	- 6.9	- 5.9	-0.5	0.0	Clamped SDTDL and SDTRL (7074)
T	-6 to +6	- 6.2	- 0.7	+1.4	+6.2	CTDL
U	-12 to 0	-12.5	- 7.4	-5.3	+0.2	CTDL
V	Any					Special
W	# 0 to -48	-53.0	- 43.0	-2.0	0.0	Relays
X	-30 to +10	-60.0	- 18.3	+5.5	+40.0	Tubes
Y	-6 to 0	- 8.8	- 5.8	-0.7	-0.1	SDTDL
Z	-6 to +6	- 7.0	- 4.2	+3.0	+6.2	Magnetic Shift Cores

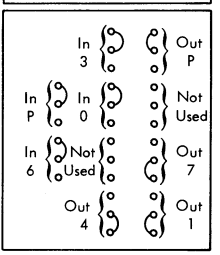
* High down level can go to +0.1 on some circuits
\# 0 to relay source voltage; typically, 0 to -48

ADDRESS CARDS

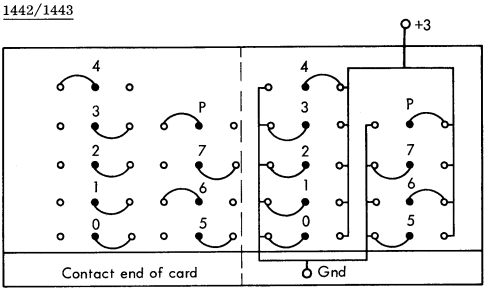
1052/2150

1. These cards located at X - X1 - D2 and X - X1 - G2
2. Groups labeled "OUT" are used to decode the bus-out lines for address match
3. Groups labeled "IN" are those which generate the address to bus-in lines
4. Jumper as shown for address "FF"
5. Maintain odd parity
6. Card part 5800529
7. See "1052-2150 Locations"





1442/1443



1. This half of card used to sample bus-out lines for address match
2. Wire from center to left for bit desired
3. Wire from center to right for all other bits
4. Maintain odd parity

1. This half used to generate address to bus-in lines
2. Wire from center to right for bits desired
3. Jumper from center to left for all other bits
4. Maintain odd parity

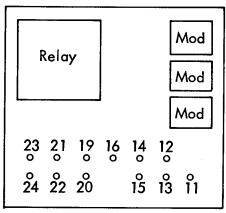
Note: Example shown above is jumpered for address 0A, card part 5804095.

Locations:
1442 - A A1 F5
1443 - A1 H06

2314

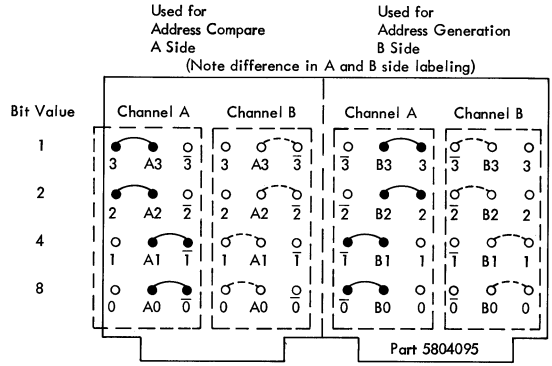
The relay card at location A-C3J3 must be jumpered to assign 2314 channel priority and allow the select out signal to be propagated.

Jumper 11 to 13, 16 to 14, 19 to 21, 22 to 24 except if lowest priority. If lowest priority, jumper 13 to 15, 21 to 23, 20 to 22 and leave jumper 16 to 14.

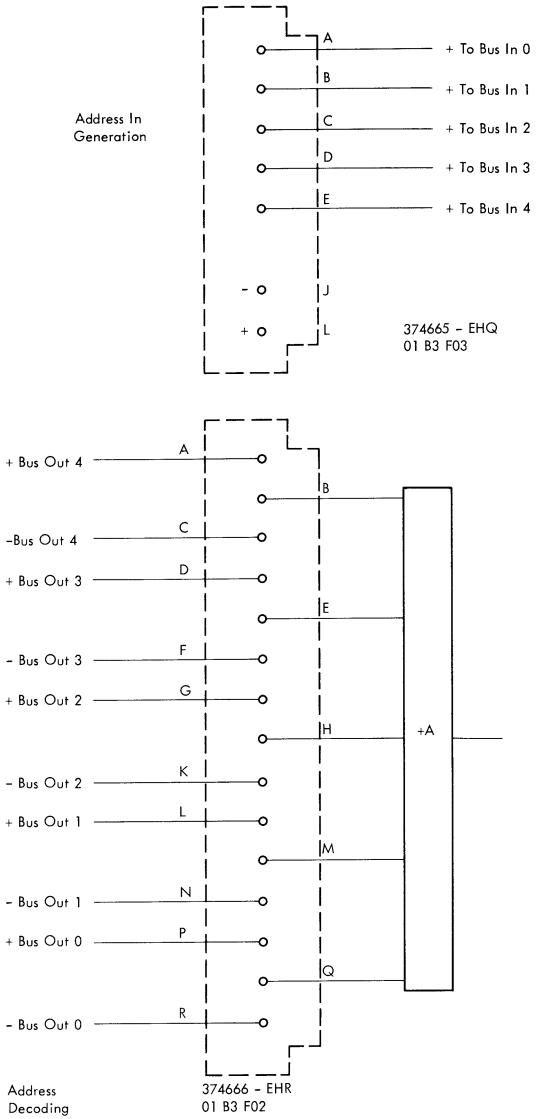


Relay card part 5801438
Use jumper part 815924
Use housing part 815923

Address select card to be set on installation with customer's address. Use jumper part 811824.



Channel A sections are to be set up on all machines. Channel B sections to be jumpered only if optional two-channel switch feature is installed. Factory built machine will ship with address 3 (0011) for channel A and address 4 (0100) for channel B.


Address In
Generation
A
B
C
D
E
J
L
+ To Bus In 0
+ To Bus In 1
+ To Bus In 2
+ To Bus In 3
+ To Bus In 4
374665 - EHQ
01 B3 F03
+ Bus Out 4
-Bus Out 4
+ Bus Out 3
- Bus Out 3
+ Bus Out 2
- Bus Out 2
+ Bus Out 1
- Bus Out 1
+ Bus Out 0
- Bus Out 0
F
G
H
K
M
N
P
Q
R
+A
Address
Decoding
374666 - EHR
01 B3 F02

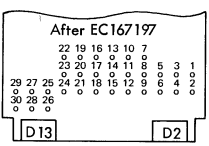
. Address and Parity Plugging

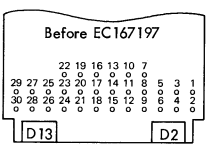
2820	Basic (AA 021)	2-Chan Feature (AA 121)
Address Card	01B-A3F3	01C-B3B4
Parity Card	01B-A3G3	01C-B3C4

Plug unit address bits on or off to output

Bit Position	Address Circuit	Bit On		Bit Off		Output	
		Post	Pin	Post	Pin	Post	Pin
P	Gen	7	D03	13	D08	10	D06
0	Gen	7	D03	13	D08	10	D06
	Comp	2	B02	6	B03	4	D02
1	Gen	8	D03	14	D08	11	B05
	Comp	30	B13	26	B12	28	D13
2	Gen	1	D03	5	D08	3	D04
	Comp	29	D12	25	B10	27	D11
3	Gen	16	D03	22	D08	19	B08
	Comp	24	D10	18	B09	21	D09
4	Gen	17	D03	23	D08	20	D07
	Comp	15	B07	9	B04	12	D05

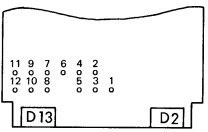
2820 Address Card Post Layout (ZZ020)
part 5800529 w/rail part 811824, or 815923 and 815924





2820 Priority Card Part 5801438
(Basic) 01B-A3D6 (2 Chan Feature) 01C-B3L6

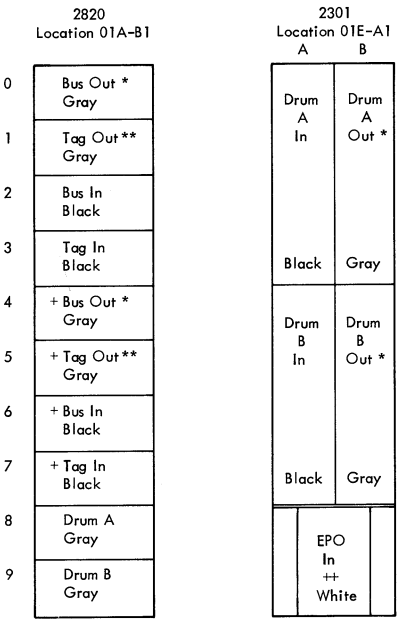
Low Priority	Normal Priority
3 to 5	1 to 3
8 to 10	7 to 9
9 to 11	10 to 12
4 to 6	4 to 6



2301 Address Plugging

Panel Jumper (Part 5700248) B1C6D07 to Address Pin			
Address	Pin	Address	Pin
0	B1B7D13	2	B1B7D11
1	B1B7B12	3	B1B7B10

Signal Cable Connectors

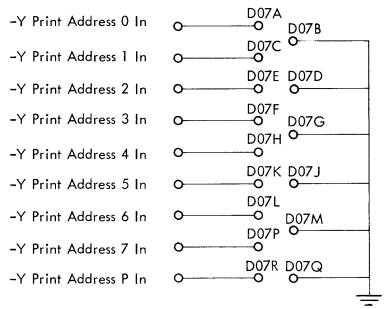


* Terminate with part 5440649 if last CU or drum on line.
** Terminate with part 5440650 if last CU on line.
\+ Dual Interface Feature.
++ 2301-2 only.

2821 Without Two-Channel Switch Feature Installed

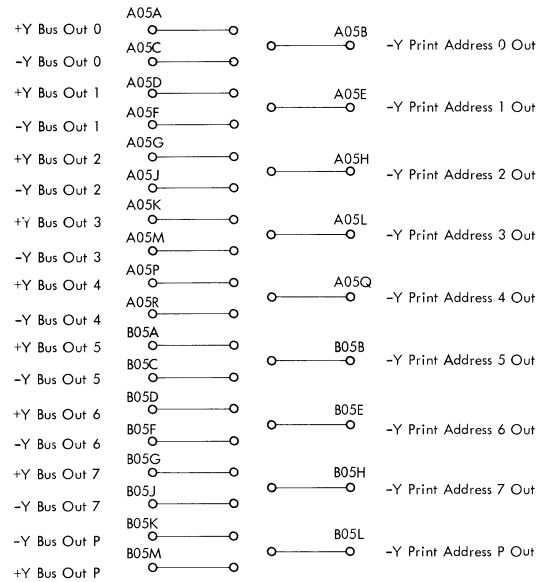
Printer Address In - Address Out

To generate address:
Allow -Y Print Address In lines to float for those bits which should be present.
Jumper other lines to ground.



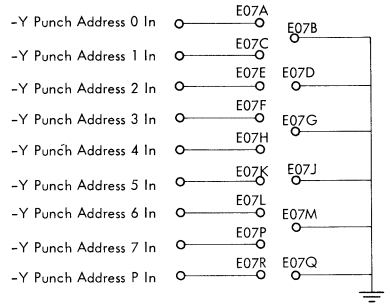
Address Out 21A3A05, B05

To recognize correct address: Jumper -Y Bus Out to -Y Print Address Out for those bits which should be present.
Jumper +Y Bus Out to -Y Print Address Out for those bits which should not be present.

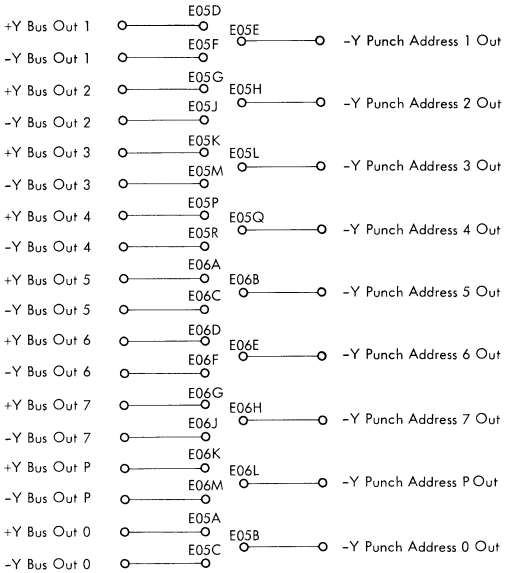


Punch Address In - Address Out (2821)

Address In 21B1E07
To generate address:
Allow -Y Punch Address In lines to float for those bits which should be present. Jumper other lines to ground.

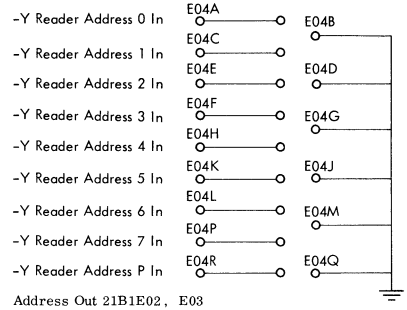


Address Out 21B1E05, E06
Jumper: -Y Bus Out to -Y Punch Address Out for those bits which should be present.
Jumper: +Y Bus Out to -Y Punch Address Out for those bits which should not be present.



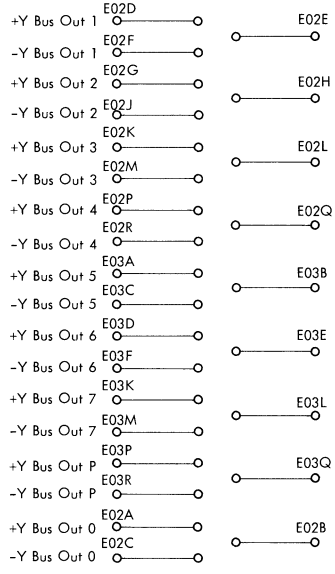
Reader Address In - Address Out (2821)

Address In 21AB1E04
To generate address:
Allow -Y Reader address In lines to float for those bits which should be present. Jumper other lines to ground.



Address Out 21B1E02, E03

To recognize correct address: Jumper -Y Bus Out to -Y Reader Address Out for those bits which should be present.
Jumper +Y Bus Out to -Y Reader Address Out for those bits which should not be present.



2821 With Two-Channel Switch Feature Installed

The TCS feature departs from the standard pattern of address-card plugging. A pluggable address card is provided for each channel, but only bits 0-4 are pluggable. These first five bits are plugged in the usual manner, and address only the control unit; thus, they can be different for each interface connection. Bits 5-7 are fixed-wired and are decoded to address the I/O device. These bits are the same for both interface connections.

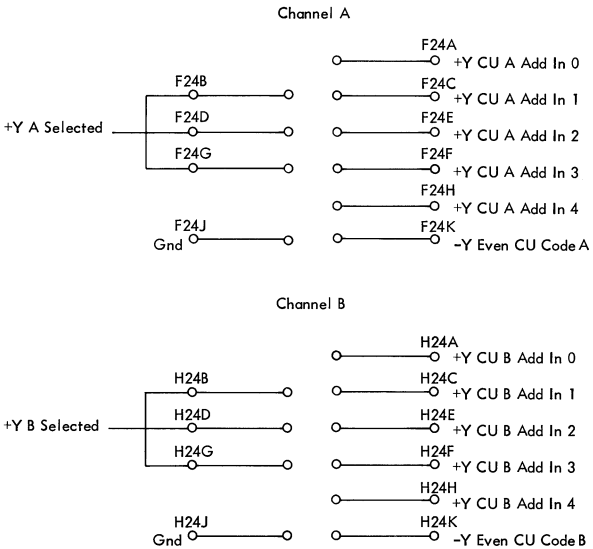
The permanent assignment of the I/O device addresses provided by wiring is:

Bits 5	6	7	I/O Device
0	0	0	Printer 1
0	0	1	Reader
0	1	0	Punch
0	1	1	Printer 2
1	0	0	Printer 3

Depending on the model of the 2821, addresses XXXXX001 through XXXXX100 for devices not present can be used for other devices on the channel.

Control Unit Address In -- Chassis 21D1

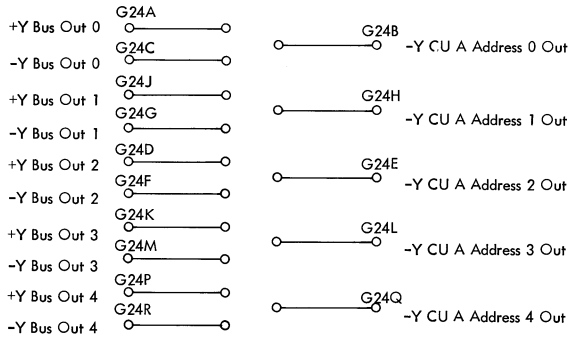
To generate correct address: For those bits which should be present, jumper +Y A selected to +Y CU add in. Allow the other address lines to float. Make the total number of jumpers on each card even by using the -Y even CU code jumper.



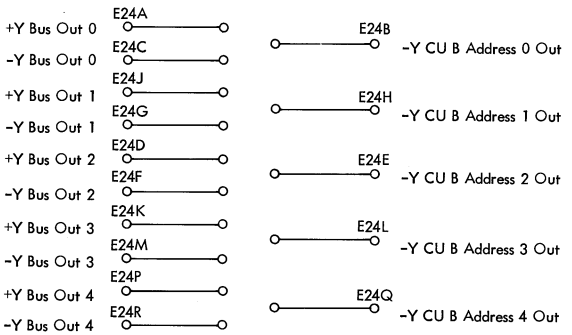
Control Unit Address Out -- Chassis 21D1

To recognize correct address:
For those bits which should be present, jumper -Y bus out to -Y CU add out.
For those bits which should not be present, jumper +Y bus out to -Y CU add out.

Channel A

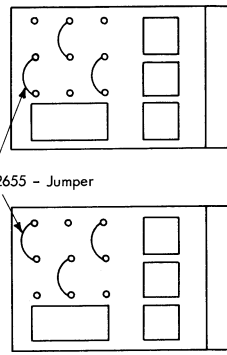


Channel B



PRIORITY JUMPER CARD

Lowest priority wire as shown at right



Highest priority wire as shown at right

Before I/O Interface EC

For 2821, SMS card YPM, part 372680:

Lowest Priority: Plug card at 21A1F09

Highest Priority: Plug card at 21A1F08

For 24XX/28XX Tape Control, SMS card EHR, part 374666:

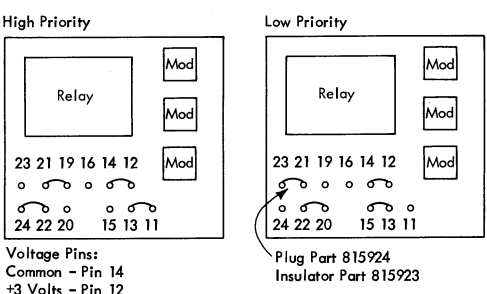
Low Priority: Plug Q→R
M→N
H→K

High Priority: Plug Q→P
M→L
H→G

Locations:

2403/2803	01A3E02	TC 40.12.2
2404/2804	01A1A13	TA 40.12.2 (IF A)
	01A1A14	TB 40.12.2 (IF B)

After I/O Interface EC



Voltage Pins:
Common - Pin 14
+3 Volts - Pin 12
+6 Volts - Pin 16

Plug Part 815924
Insulator Part 815923

Select Out Bypass
Part 5801438

OPERATOR PANEL

OPERATOR PANEL INDICATORS

System Operating	Manual	Wait	CPU	I/O
Off	Off	Off	Invalid with Power on	
Off	Off	On	Waiting	Not Operating
Off	On	Off	Stopped	Not Operating
Off	On	On	Stopped and Waiting	Not Operating
* On	Off	Off	Running	Undetermined
* On	Off	On	Waiting	Operating
* On	On	Off	Stopped	Operating
* On	On	On	Stopped and Waiting	Operating

* Customer/CE meter should be operating.

1052 PRINTER-KEYBOARD

Commands

Command	Bit 0	1	2	3	4	5	6	7
Write without Carrier Return	0	0	0	0	0	0	0	1
Write with Carrier Return	0	0	0	0	1	0	0	1
Read	0	0	0	0	1	0	1	0
Control Alarm	0	0	0	0	1	0	1	1
No-op	0	0	0	0	0	0	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	1	0	0

Status Byte

Bit	Name	Description
0	Attention	Request Button
1	Not Used	
2	Not Used	
3	Busy	
4	Channel End	
5	Device End	
6	Unit Check	Defined by Sense Byte
7	Unit Exception	Read Cancel Button

Sense Byte

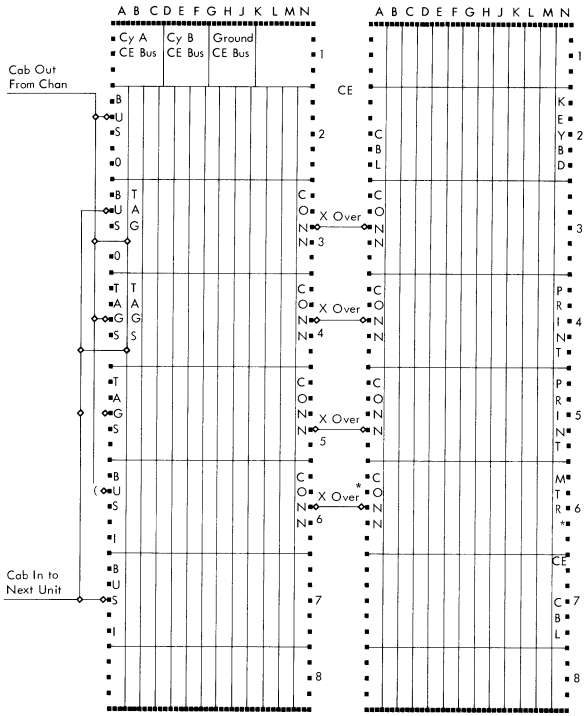
Bit	Name	Description
0	Command Reject	Invalid Command
1	Intervention Required	Not Ready
2	Bus-Out Check	Parity Error on Bus Out
3	Equipment Check	Typewriter Parity Error

X Board	
System	Location
2040	01BC1
2050	01CD4
2060	01ED1
2150	01AB1

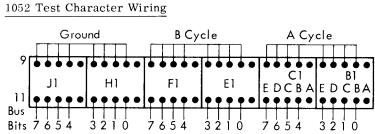
X Board (Card Side)

Y Board	
System	Location
2040	01BD1
2050	01CE4
2060	01EE1
2150	01AC1

Y Board (Card Side)



1052 Test Character Wiring



Bus	A Cycle	B Cycle
0	1	1
1	0	1
2	1	0
3	0	1
4	0	0
5	1	1
6	1	0
7	0	0

Desired EBCDIC character and/or 1052 control function goes in this chart for layout purposes

After layout:

	-On Back Panel-		-On Back Panel-
If AB = 00 (EX 4, 7)	Jumper Corresponding Bus Position to Ground	If AB = 10 (EX 2, 6)	Jumper Corresponding Bus Position to A Cycle "W" "M"
If AB = 01 (EX 1, 3)	Jumper Corresponding Bus Position to B Cycle	If AB = 11 (EX 0, 5)	Leave Bus Pos. Open

BA 84 21 6 Bit Code	LC	Print/ Function	01 23 45 67 8 Bit Code	UC	Print/ Function	01 23 45 67 8 Bit Code
00 00 01	1	1	11 11 00 01	=	=	01 11 11 10
00 00 10	2	2	11 11 00 10	<	<	01 00 11 00
00 00 11	3	3	11 11 00 11	;	;	01 01 11 10
00 01 00	4	4	11 11 01 00	:	:	01 11 10 10
00 01 01	5	5	11 11 01 01	%	%	01 10 11 00
00 01 10	6	6	11 11 01 10	'	'	01 11 11 01
00 01 11	7	7	11 11 01 11	>	>	01 10 11 10
00 10 00	8	8	11 11 10 00	*	*	01 01 11 00
00 10 01	9	9	11 11 10 01	(	(	01 00 11 01
00 10 10	0	0	11 11 00 00	)	)	01 01 11 01
11 00 01	a	a	10 00 00 01	A	A	11 00 00 01
11 00 10	b	b	10 00 00 10	B	B	11 00 00 10
11 00 11	c	c	10 00 00 11	C	C	11 00 00 11
11 01 00	d	d	10 00 01 00	D	D	11 00 01 00
11 01 01	e	e	10 00 01 01	E	E	11 00 01 01
11 01 10	f	f	10 00 01 10	F	F	11 00 01 10
11 01 11	g	g	10 00 01 11	G	G	11 00 01 11
11 10 00	h	h	10 00 10 00	H	H	11 00 10 00
11 10 01	i	i	10 00 10 01	I	I	11 00 10 01
10 00 01	j	j	10 01 00 01	J	J	11 01 00 01
10 00 10	k	k	10 01 00 10	K	K	11 01 00 10
10 00 11	l	l	10 01 00 11	L	L	11 01 00 11
10 01 00	m	m	10 01 01 00	M	M	11 01 01 00
10 01 01	n	n	10 01 01 01	N	N	11 01 01 01
10 01 10	o	o	10 01 01 10	O	O	11 01 01 10

BA 84 21 6 Bit Code	LC	Print/ Function	01 23 45 67 8 Bit Code	UC	Print/ Function	01 23 45 67 8 Bit Code
10 01 11	p	p	10 01 01 11	P	P	11 01 01 11
10 10 00	q	q	10 01 10 00	Q	Q	11 01 10 00
10 10 01	r	r	10 01 10 01	R	R	11 01 10 01
01 00 10	s	s	10 10 00 10	S	S	11 10 00 10
01 00 11	t	t	10 10 00 11	T	T	11 10 00 11
01 01 00	u	u	10 10 01 00	U	U	11 10 01 00
01 01 01	v	v	10 10 01 01	V	V	11 10 01 01
01 01 10	w	w	10 10 01 10	W	W	11 10 01 10
01 01 11	x	x	10 10 01 11	X	X	11 10 01 11
01 10 00	y	y	10 10 10 00	Y	Y	11 10 10 00
01 10 01	z	z	10 10 10 01	Z	Z	11 10 10 01
10 00 00	-	-	01 10 00 00	—	¬	01 10 11 01
11 00 00	&	&	01 01 00 00	+	+	01 00 11 10
01 00 00	@	@	01 11 11 00	¢	¢	01 00 10 10
10 10 11	$	$	01 01 10 11	!	!	01 01 10 10
00 10 11	#	#	01 11 10 11	"	"	01 11 11 11
01 10 11	,	,	01 10 10 11	|	¬	01 00 11 11
11 10 11	.	.	01 00 10 11	¬	¬	01 01 11 11
01 00 01	/	/	01 10 00 01	?	?	01 10 11 11
11 11 01	Tab	Tab	00 00 01 01	TAB	TAB	00 00 01 01
10 11 10	Bksp	Backspace	00 01 01 10	Bksp	Backspace	00 01 01 10
01 11 01	LF	Line Feed	00 10 01 01	LF	Line Feed	00 10 01 01
00 00 00	SP	Space	01 00 00 00	SP	Space	01 00 00 00
10 11 01	NL	New Line	00 01 01 01	NL	New Line	00 01 01 01

Commands

Command	P	0	1	2	3	4	5	6	7
	Bit								
Test I/O	1	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	0	1	0	0
Read Backwards	P	0	0	M	M	1	1	0	0
Write (Diag Only)	0	0	0	0	0	0	0	0	1
Read	P	0	0	M	M	0	0	1	0
Control	P	M	M	M	M	1	1	1	1
No Op	1	0	0	0	0	0	0	1	1

Control Commands

Command	P	0	1	2	3	4	5	6	7	
	Bit									
Select Stacker A	1	1	0	1	0	1	1	1	1	
B	0	1	0	1	1	1	1	1	1	
0	1	0	0	0	0	1	1	1	1	
1	0	0	0	0	1	1	1	1	1	
2	0	0	0	1	0	1	1	1	1	
3	1	0	0	1	1	1	1	1	1	
4	0	0	1	0	0	1	1	1	1	
5	1	0	1	0	1	1	1	1	1	
6	1	0	1	1	0	1	1	1	1	
7	0	0	1	1	1	1	1	1	1	
8	0	1	0	0	0	1	1	1	1	
9	1	1	0	0	1	1	1	1	1	
R	1	1	1	0	0	1	1	1	1	
Pocket Light Control	1	1	1	1	1	1	1	1	1	(1419 Only)
Engage	0	1	1	1	0	1	1	1	1	
Disengage	0	1	1	0	1	1	1	1	1	

1419 Status Byte

The single address and dual address adapters use the same status byte format except as noted. There are separate status bytes for the primary and secondary control units on dual address machines.

Bit	Name	Meaning
0		Not Used
1		Not Used
2		Not Used
3	Busy	Control unit and device busy to all commands except test I/O.
4	Channel End	Control unit may be disconnected from the interface.

1419 Status Byte (Continued)

Bit	Name	Meaning
5	Device End	Machine has completed a command.
6	Unit Check	Set by command reject, intervention required, bus out check, auto select, data check, or overrun.
7	Unit Exception	Read command has been given but there are no documents between the separator and PDS6 and the separator is off. (This bit is not used in the SCU status byte.)

1412 SAA Sense Byte 1

Bit	Name	Meaning
0	Command Reject	Two read commands without intervening stacker select; stacker select command on an auto select document. If stacker select is accepted and another is issued for same document, invalid control command or a write command.
1	Intervention Required	Jam, motor not running, film stop, full pocket, empty hopper or sort compare.
2	Bus Out Check	Bus out parity error.
3		Not Used
4	Data Check	Select field not read correctly.
5	Overrun	Channel did not accept character in allotted time.
6	Late Read	Document under read head without read backward command.
7	Document Spacing Error	Document spacing too small or document too long.

1412 SAA Sense Byte 2

Bit	Name	Meaning
0		Not Used
1		Not Used
2		Not Used
3	Amount Field Error	Unreadable character, special symbol missing or sequence error, field missing and read field key depressed, overrun in field, field length invalid, and late read indicator on.
4	Process Control Field Error	
5	Account Number Field Error	
6	Transit Routing Field Error	
7	Serial Number Field Error	

1419 SAA Sense Byte 1

Bit	Name	Meaning
0	Command Reject	Two reads without an intervening stacker select; a stacker select issued for an auto-select document. If a stacker select is accepted and another is issued for same document, invalid control command and a write command when not in diagnostic mode.
1	Intervention Required	Jam, motor not running, film stop, full pocket, empty hopper, sort compare or endorser stop condition.
2	Bus Out Check	Bus out parity error.
3		Not Used
4	Data Check	Selected field not read correctly.
5	Overrun	Character not accepted in allotted time and late stacker select command.
6	Auto Select	Document rejected because late read, document spacing and overlength errors.
7	Document Spacing	Document spacing error (pre-sort machines only).

1419 SAA--SAA and DAA, PCU Sense Byte 2

Bit	Name	Meaning
0		Not Used
1		Not Used
2	Document under Read Head	Set on or off depending on location of document when sense command is given.
3	Amount Field Valid	Field is read without error, including symbols, when read field key is operated.
4	Process Control Field Valid	
5	Account Number Field Valid	
6	Transit Field Valid	
7	Serial Number Field Valid	

1419 DAA -- PCU Sense Byte 1

Bit	Name	Description
0	Command Reject	Write command when not in diagnostic mode; invalid command; read command with modifier bit 2 or 3 when machine is not in 1419 sort mode.
1	Intervention Required	Jam, motor not running, film stop, full pocket, sort check, endorser stop, B/N advance check stop.
2	Bus Out Check	Bus out parity check.
3		Not Used.
4	Data Check	Selected field not read correctly.
5	Overrun	Channel did not accept character in allotted time.
6	Auto Select	Document spacing error.
7		Not Used.

1419 DAA -- PCU Sense Byte 2

(Same as 1419 SAA Sense Byte 2)

SCU -- Sense Byte 1

Bit	Name	Description
0	Command Reject	Two stacker select commands between external interrupts; stacker select command before first external interrupt or with document still under read head. Batch numbering advance or pocket light control command with the feature uninstalled; invalid command.
1	Intervention Required	Same as PCU sense byte 1, bit 1.
2	Bus Out Check	Bus out parity error.
3		Not Used.
4		Not Used.
5	Late Stacker Select	Stacker select command issued to a document past the selector station.
6	Auto Select	Set to a stacker select command issued to an auto select document.
7	Operator Attention	A batch numbering update command issued with the batch numbering switch off.

1442 CARD READ PUNCH

Commands

Command	Bit 0	1	2	3	4	5	6	7
Read	M	M	M	0	0	0	1	0
Write	M	M	M	0	0	0	0	1
Control	M	M	0	0	0	0	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense	x	x	0	0	0	1	0	0
No-Op	0	0	x	x	x	x	1	1
Punch Diag	x	x	1	1	0	1	0	0
Read Diag	x	x	0	1	0	1	0	0
Modifiers								
Eject	1	M	M	M	x	-	-	-
Select Stacker 2	M	1	M	M	x	-	-	-
Card Image	M	M	1	M	x	x	-	-
1400 Mode	M	M	M	1				

x is "don't care" bit

Status Byte

Bit	Name	Description
3	Busy	
4	Channel End	
5	Device End	
6	Unit Check	-- further explained by sense byte
7	Unit Exception	-- EOF and last card has been read

Sense Byte

Bit	Name	Description
0	Command Reject	
1	Intervention Required	-- not ready
2	Bus-Out Check	
3	Equipment Check	-- reader check, punch check, invalid card code punched and data error on CE read or write.
4	Data Check	-- invalid card code on read
5	Overrun Check	

Commands

Command	Bit 0	1	2	3	4	5	6	7
Write	M	M	M	M	M	0	0	1
Control (Skip or Space)	M	M	M	M	M	0	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense	0	0	0	0	0	1	0	0
Diagnostic Read	0	0	0	0	1	1	0	0
Diagnostic Write	1	0	0	0	1	1	0	1
Diagnostic Control	1	0	1	1	0	1	1	1

Modifiers for Write and Control

Operation	Bit 0	1	2	3	4
Space 1 Line	0	0	0	0	1
Space 2 Lines	0	0	0	1	0
Space 3 Lines	0	0	0	1	1
Skip to Channel 1	1	0	0	0	1
Skip to Channel 2	1	0	0	1	0
Skip to Channel 12	1	1	1	0	0

Carriage Operation on a Write is a space or skip after print. On a Control, it is an immediate.

Status Byte

Bit	Name	Description
0, 1, 2		Not Used
3	Busy	Command stored or status stacked.
4	Channel End	
5	Device End	
6	Unit Check	Channel 9 sensed in carriage tape.
7	Unit Exception	Channel 12 sensed in carriage tape.

Sense Byte

Bit	Name	Description
0	Command Reject	Because read-backward command was received, or because more than 3 line spaces were requested, or because skip to channel 0, 13, 14, or 15 was received.
1	Intervention Required	Printer not ready because forms check ran out or jammed, or stop key or carriage stop key pressed, or cover interlock open or ribbon check (1445 N1 only; end of MICR ribbon sensed).
2	Bus-Out Check	Parity error on bus-out during initial selection with command-out tag up, or data transfer with service-out tag up.
3	Equipment Check	Printer malfunction because of buffer register parity error or typebar synchronization error.
4 & 5	Typebar Selection	Changed only by repositioning the typebar-character indicator switch. 0 0 52-character set 0 1 13-character set 1 0 39-character set 1 1 63-character set
6		Not Used
7	Channel 12	Hole sensed in channel 9 of carriage control tape during last write or control command.

Commands	Bit 0	1	2	3	4	5	6	7	Hex	Options Required
Control										
No Operation	0	0	0	0	0	0	1	1	03	
Set BAC and Stop	0	0	0	0	0	1	1	1	07	1
Set Audible Alarm	0	0	0	0	1	0	1	1	0B	
Insert Cursor	0	0	0	0	1	1	1	1	0F	2
Set Prog Fcn Indicators	0	0	0	1	1	0	1	1	1B	3
Remove Cursor	0	0	0	1	1	1	1	1	1F	2
Set BAC and Start	0	0	1	0	0	1	1	1	27	1
Write	0	0	0	0	0	0	0	1	01	
Read										
Read Direct	0	0	0	0	0	0	1	0	02	
Read Buffer	0	0	0	0	0	0	1	0	02	1
Read Cursor	0	0	0	0	0	1	1	0	06	2
Read Manual Input	0	0	0	0	1	1	1	0	0E	4
Read X-Y	0	0	0	1	0	0	1	0	12	
Sense										
Test I/O	0	0	0	0	0	0	0	0	00	
Sense	0	0	0	0	0	1	0	0	04	

Note: Option Codes - 1 - Buffer
2 - Buffer, Character Generator and A/N Keyboard
3 - Program Function Keyboard
4 - Alpha/Numeric or Program Function Keyboard

Summary of Status and Sense Information

Status Byte

Bit	Name
0	Attention
1, 2	Unused
3	Busy
4	Chan End
5	Device End
6	Unit Check
7	Unused

Sense Byte 0

Bit	Name
0	Command Reject
1	Intervention Required
2	Bus Out Check
3	Unused
4	Data Check
5	Unused
6	Buffer Running
7	Unused

Sense Byte 1

Bit	Name
0	Light Pen Detect
1	End Order Sequence
2	Character Mode
3-7	Unused

Sense Byte 2

Bit	Name
0, 1, 2	Unused
3-7	Hi-order Buffer Address Ctr

Sense Byte 3

Bit	Name
0-5	Lo-order Buffer Address Ctr
6	BAC, value 2
7	BAC, value 1

Note: Sense bytes 2 and 3 will be meaningless if buffer is running when sense command is issued.

Command Decoding

Channel Command	2702 Command	Command Byte Input to 2702 (Bus In)								LCW Command Field				LCW Mode Field			LCW TC Field	
		P	0	1	2	3	4	5	6	7	4	5	6	7	4	2	1	2	1
Sense	Sense	0	0	0	0	0	0	1	0	0	0	1	0	0					
Write	Write	0	0	0	0	0	0	0	0	1	0	0	0	1					
	Auto Wrap	1	0	0	0	0	0	1	0	1	0	1	0	1					
	Dial*	0	0	0	1	0	1	0	0	1	0	0	1	1	0	1	0		
	Break	0	0	0	0	0	1	1	0	1	1	1	0	1					
	Poll	1	0	0	0	0	1	0	0	1	1	0	0	1					
Read	Read	0	0	0	0	0	0	0	1	0	0	0	1	0					
	Prep Rd	1	0	0	0	0	0	1	1	0	0	1	1	0					
	Inhibit	1	0	0	0	0	1	0	1	0	1	0	1	0					
	Search	0	0	0	0	0	1	1	1	0	1	1	1	0					
Control	SADZER	0	0	0	0	1	0	0	1	1	0	0	1	1	0	0	0	0	0
	SADONE	1	0	0	0	1	0	1	1	1	0	0	1	1	0	0	0	0	1
	SADTWO	1	0	0	0	1	1	0	1	1	0	0	1	1	0	0	0	1	0
	SADTHREE	0	0	0	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1
	Enable	1	0	0	1	0	0	1	1	1	0	0	1	1	0	0	1		
	Disable	0	0	0	1	0	1	1	1	1	0	0	1	1	0	1	1		
	No-Op	1	0	0	0	0	0	0	1	1									
	Pseudo**										1	1	1	1					

* Decoded by channel as write command and by 2702 as control command.
** Stack from channel.

Note: Information on the IBM 2701 DAU may be found in the Field Engineering Maintenance Diagrams Manual, IBM 2701 Data Adapter Unit, Form Y27-2020. Information on the IBM 2703 may be found in the Field Engineering Handbook, IBM 2703 Transmission Control, Form Y27-0033.

Mode Control Codes from Control-Type Command, Bits 3, 4, and 5

Mode Name	Mode Field Position		
	4	2	1
No further definition required	0	0	0
Enable	0	0	1
Dial	0	1	0
Disable	0	1	1

Mode Control Codes from Terminal Controls

Mode Field Pos.	Mode Name			
	IBM Type I	IBM Type II	TTY Type I	TTY Type II
000	Control Mode	Control Mode	LTRS Mode	Not Used
001	Text In Downshift Mode	Text In Mode	FIGS Mode	
010	Text Out Downshift Mode	Text Out Mode	LTRS Search Mode	
011	Not Used	Not Used	FIGS Search Mode	
100	Not Used	Not Used	Not Used	
101	Text In Upshift Mode	Not Used	Not Used	
110	Text Out Upshift Mode	Not Used	Not Used	
111	Not Used	Not Used	Not Used	

Sequence Control Cards

Sequence Field Position			IBM Terminal Control Type I		IBM Terminal Control Type II		TTY Terminal Control Type I WTC Terminal Control		TTY Terminal Control Type II	
4	2	1	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit
0	0	0	Reset	Reset	Reset	Reset	Reset	Reset	Reset	Reset
0	0	1	Not Used	Data	Not Used	Data	Data	Data	Not Used	Data
0	1	0	Receiving	Halt	Receiving	Halt	Receiving	Halt	Receiving	Halt
0	1	1	Timeout	Prep End	Timeout	Prep End	Timeout	Prep End	Timeout	Prep End
1	0	0	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
1	0	1	LRC	LRC	Not Used	Not Used	FIGS H	Not Used	Not Used	Not Used
1	1	0	Not Used	Not Used	Not Used	Not Used	A	Not Used	Not Used	Not Used
1	1	1	End	End	End	End	End	End	End	End

Status Bytes (Initial and Ending)

Bit	Name	Description
0	Attention	(2702 does not set this bit in the status byte).
1	Status Modifier	Test I/O instruction decoded on initial selection. Unit busy or machine reset (power on, manual, or interface reset) while in initial selection.
2	Control Unit End	Unit busy or machine reset while in initial selection.
3	Busy	Unit busy or machine reset while in initial selection.
4	Channel End	No-op decoded during initial selection. Receive operation in progress when write-type command is about to be inserted. End sequence set in a send/receive operation.
5	Decode End	No-op decoded during initial selection. Receive operation in progress when write-type command is about to be inserted. End sequence set in a send/receive operation.
6	Unit Check	If stacked on initial selection and other than Test I/O or No-op.
7	Unit Exception	Parity check on command byte during initial selection. Invalid command byte decoded during initial selection. Channel End and Device End (4 and 5) and one of the following: not operate, equipment check, bus-out parity, timeout, overrun, command reject, and data check. Receive operation in progress when write-type command is about to be inserted. End sequence on a write poll command. EOT received while in sequence 2 of a read command. Negative answer to poll from 1050 in control mode of a receive operation.

Sense Byte

Bit	Name	Description
0	Command Reject	Invalid command decoded during initial selection.
1	Intervention Required	Phone line becomes not operational during a read or write operation in other than sequence 0 or 7.
2	Bus-Out Parity Check	Parity check detected (during initial selection) in command byte. Parity check detected during service cycle.
3	Equipment Check	Serial data bit and line adapter transmitter do not match (write operations only). Initial selection and command already stored. Enable and disable command not executed.
4	Data Check	Terminal controls signaled stop time for a character (in read operation only), but the line was not in mark state. VRC check, LRC check, (N) response to a message, stop bit error, echo check on TTY.
5	Overrun	In read operation, one character (or more) was destroyed because channel failed to service when required.
6	Receiving	Timeout in progress, and space is received. As long as command field does not hold control code, space is received and bit count and strobe count fields are all 0's. Stop from channel or halt I/O while in receive control.
7	Timeout	Timeout 28 sec (strobe count and bit count fields are all 1's) in modes 001 and 101 of read operation. Timeout 2 sec in mode 000 of read operation.

2800/2400 Feature Summary

FAA	RPQ for Federal Aviation Agency machines.
MIS	Multiple interface switch. Allows two-channel operation of 2803/2403; manual or program controlled.
7TRK	Allows TCU to handle Models 1, 2, 3 NRZI seven-track MTU.
9TRK	Allows TCU to handle Models 1, 2, 3 NRZI nine-track MTU.
NRZI	Companion feature with seven- or nine-track compatibility.
Model Compatibility	Allows Models 1, 2, 3 to run on Model 2 TCUs.
Dual Density	Allows Models 4, 5, 6 to run in nine-track NRZI mode.
SIMS	Simultaneous read while write. Available on Models 1, 2, 3, 4, 5, 6 tape drives and Models 1 and 2 TCUs.
SXT	Sixteen address feature. Allows operation of 16 tape drives on one TCU.
DC	Data convert. Allows seven-track binary conversion to nine-bit bytes.

Commands

Command Code	0	1	2	3	4	5	6	7	
Write	0	0	0	0	0	0	0	1	
Read	0	0	0	0	0	0	1	0	
Read Backward	0	0	0	0	1	1	0	0	
Sense	0	0	0	0	0	1	0	0	
Control	0	0	C	C	C	1	1	1	(Tape motion operation)
	D	D	M	M	M	0	1	1	(7-track mode setting op)
	1	1	N	N	N	0	1	1	(9-track mode setting op, Models 4-6; NOP for Mod 1-3)

C	C	C	(Control Code)
0	0	0	Rewind (REW)
0	0	1	Rewind and Unload (RUN)
0	1	0	Erase Gap (ERG)
0	1	1	Write Tape Mark (WTM)
1	0	0	Backspace Block (BSB)
1	0	1	Backspace File (BSF)
1	1	0	Forward Space Block (FSB)
1	1	1	Forward Space File (FSF)

*N	N	N	
0	0	0	1,600 bpi PE reset condition
0	0	1	800 bpi NRZI

* Other bit patterns in this group are reserved for future use.

D	D	(Density Set) -- Seven-Track Operation Only	
0	0	200 bpi	Seven-Track
0	1	556 bpi	
1	0	800 bpi reset condition	
1	1	Set nine-track mode, Models 4-6	

Note: Nine-track operation overrides but does not reset a seven-track mode setting. Seven-track operation overrides but does not reset a nine-track mode setting. Nine-track operations on Models 1, 2, and 3 force 800 bpi and odd parity.

M	M	M	(Mode Modifiers)
0	0	0	NOP (No operation)
0	0	1	Reserved for diagnostic use only
0	1	0	Set density; set odd parity; data converter on (Note 1); translator off. Reset condition (Note 2).
0	1	1	Request track in error (TIE). Nine-track NRZI only; (Request TIE issued to a Model 4, 5, 6, 7, PE or 2415 results in NOP).
1	0	0	Set density; set even parity; data converter off; translator off.
1	0	1	Set density; set even parity; data converter off; translator on.
1	1	0	Set density; set odd parity; data converter off; translator off. Reset condition if data converter feature is not installed with the seven-track feature.
1	1	1	Set density; set odd parity; data converter off; translator on.

Notes:

1. A read backward command overrides data converter on mode set.

2. Reset condition if data converter feature is installed with the seven-track feature. This command will be rejected by control units that have the seven-track feature, but do not have the data converter feature installed. Density, odd parity, and translator off will be set.

Status Byte

Bit	Name	Description
0	Attention	Not used.
1	Status Modifier	Present with busy to indicate TCU busy.
2	Control Unit End	Signaled by the TCU: (a) At completion of operations during which a TCU busy was indicated. (b) At the completion of a control immediate operation during which a unit check or unit exception is detected.
3	Busy	When presented without bit 1 (status modifier bit), indicates that the tape unit is busy.
4	Channel End	Indicates that a read, read backward, write, mode set or sense has been completed, or that a control command has been accepted.
5	Device End	Indicates that the tape unit has completed operation at TU level of command. Device end indicated with channel end at the completion of command.
6	Unit Check	Set whenever: (a) Any bit is on in sense byte 0. (b) Tape unit performing read backward, backspace record or backspace file into or at load point. (c) A rewind and unload is completed at the TCU level.
7	Unit Exception	Set when: (a) A write, WTM or ERG operation is performed in the end of tape area. (b) A tape mark is sensed during a read, read backward, forward space record, or backspace record.

Sense Byte 0

Bit	Designation	2401–2404, 2415 and 2420 Interpretation	
		Models 1–3 (and Models 4–6, 800 bpi, NRZI Mode)	Models 4–7 (1,600 bpi, PE)
0	Command reject	Set when a write, write tape mark, or erase command is addressed to a file protected tape unit, or a data-converter-on control command that is addressed to a seven-track tape unit is recognized on a TCU with the seven-track compatibility feature but without the data converter feature. In this case, mode set is executed for parity, density, and translator.	Same as Models 1–3
1	Intervention required	Set whenever tape unit status A is inactive, i.e., tape unit is not ready or nonexistent. See "Sense Byte 1."	Same as Models 1–3
2	Bus-out check	Set whenever even parity appears on the information bus lines from the channel to the control unit.	Same as Models 1–3
3	Equipment check (excluding 2415) Equipment check (2415)	Set when reject tape unit (bit 1, byte 4) or sequence error (bit 5, 6, or 7 of byte 4) is set. Set whenever C-compare or clock check occurs. See "Sense Byte 3."	Set when reject tape unit (bit 1, byte 4) is set. Same as Models 1–3
4	Data check	Set when a data check occurs. See "Sense Byte 3."	Same as Models 1–3; see "Sense Byte 4."
5	Overrun	Set if service is requested, but data cannot be transferred during a read, write, or read backward operation. Data transfer stops as soon as condition is detected. Note: Data check during overrun suppresses the overrun indication.	Same as Models 1–3
6	Word count zero	Set during a write operation if transfer of data is prevented before the first byte of data. When word count zero is set, no tape motion occurs.	Same as Models 1–3
7	Data converter check	See "Data Conversion Feature."	Same as Models 1–3

Sense Byte 1

Bit	Designation	2401-2404, 2415 and 2420 Interpretation	
		Models 1-3 (and Models 4-6, 800 bpi, NRZI Mode)	Models 4-7 (1,600 bpi, PE)
0	Noise (excluding 2415)	During a read forward space block, indicates that data was recognized after the normal LRC byte time but not long enough after to be considered a new block. Data before the LRC byte is checked and transferred; data after the LRC byte turns on the noise bit and maintains tape motion, but is not transferred. When connected to Model 2 control, during a read backward or backspace block, if data is recognized after the disconnect sequence is started. With Model 1 control, data recognized after start of disconnect, is transferred as part of block. Noise bit is not set; data check is probable.	Set during read or read backward if a data check occurs.
		During a write, erase gap, or write tape mark, indicates that data (or noise caused by tape defects) was detected at the read head before the block or tape mark was written, or during erase gap while the tape was being erased. Data check and unit check are indicated.	Same as Models 1-3
0	Noise (2415)	During a write or write tape mark, indicates that data (or noise caused by tape defects) was detected at the read head before the block or tape mark was written.	Same as Models 1-3
1*	TU Status A	Selected and ready.	Same as Models 1-3
2*	TU Status B (non-2415)	Not ready, or rewinding, or under the control of another TCU via the 2816 Switching Unit. Assuming no outstanding device end status, the bits determine response to initial selection as follows:	Same as Models 1-3

<table>
<tr><td>2*</td><td>TU Status B</td><td>
<table>
<tr><th>Tape Unit Status A</th><th>Tape Unit Status B</th><th>Tape Unit Status</th><th>Response to Initial Selections</th></tr>
<tr><td>0</td><td>0</td><td>Nonexistent</td><td>Unit check</td></tr>
<tr><td>0</td><td>1</td><td>Not ready</td><td>Unit check, arm for device end</td></tr>
<tr><td>1</td><td>0</td><td>Ready and not rewinding and not switched.*</td><td>Clear status</td></tr>
<tr><td>1</td><td>1</td><td>Ready and rewinding or switched or power is down on a tape unit attached through a switching unit.</td><td>Busy, arm for device end</td></tr>
</table>
<u>Note:</u> Unit check is not signaled for a sense operation. Following unit check or busy indication, device end will be signaled when the tape unit becomes ready and not rewinding.
(2415) No references to the 2816 Switching Unit apply.</td><td></td></tr>
<tr><td>3</td><td>Seven-track</td><td>The selected tape unit has the seven-track feature installed.</td><td>Same for 2415
Always 0 for 2401-2403 Models 4-7.</td></tr>
<tr><td>4</td><td>Load point</td><td>The selected tape unit is at load point.</td><td>Same as Models 1-3</td></tr>
<tr><td>5</td><td>Selected and write status</td><td>The selected tape unit is in write status.</td><td>Same as Models 1-3</td></tr>
<tr><td>6</td><td>File protect</td><td>The selected tape unit is in file protect status</td><td>Same as Models 1-3</td></tr>
<tr><td>7</td><td>Not capable</td><td>Not used, always set to zero.</td><td>Tape unit and/or control are not compatible with mounted tape (indicated after read from load point).</td></tr>
<tr><td colspan="4">* Switched means that the tape unit is selected by some other control unit under control of a tape unit switch.</td></tr>
</table>

Sense Byte 2

2401-2404, 2415 and 2420 Interpretation	
Models 1-3 (and Models 4-6, 800 bpi, NRZI Mode)	Models 4-7 (1,600 bpi, PE)
This sense byte contains the track-in-error indicator bits that are set at the end of a read or read backward command if a data check has been encountered. See "Cyclic Redundancy Check." At the end of a properly executed read or read backward with no data check and at the end of all other commands, sense byte 2 contains at least bits 6 and 7 set to 1's. No error correction is attempted when operating with seven-track tape units; bits 6 and 7 are set to 1's in sense byte 2.	Not applicable
2415: Not applicable; bits 6 and 7 set to 1 unconditionally.	

Sense Byte 3

Bit	Designation	2401-2404, 2415 and 2420 Interpretation	
		Models 1-3 (and Models 4-6, 800 bpi, NRZI Mode)	Models 4-7 (1,600 bpi, PE)
0	R/W VRC (2401-4 Models 1-6) Data reg VRC (2415 Models 1-6)	A vertical redundancy check occurred during a read or read backward operation. Indicator is not set after an overrun or after receipt of a stop signal. *	A vertical parity error occurred during read or read backward operation that could not be corrected, or a Model 7 write operation.
1	LRCR (Models 1-3) Multiple Track Error (Models 4-6)	A longitudinal redundancy check occurred during write, write tape mark, read, or read backward operation.	Weak signal in more than one track on a read or read backward operation. Data is incorrect. Also velocity check on write operation.

2	Skew	Excessive skew detected by a read back check during a write, write tape mark, or erase operation.	Excessive skew detected during a read or read backward operation.
3	CRC (Models 1-3) End data check (Models 4-6)	A cyclic redundancy check occurred during a read or read backward operation (nine-track only). 2415: Not applicable.	Set when sync burst following data block is not properly recognized, or is improperly recognized before actual end of data. 2415: Set with false end-of-block indication.
4	Skew reg VRC (Models 1-3) Envelope check (Models 4-6)	A character with incorrect parity detected in skew register during write, write tape mark, or erase operation.	Indicates at least one track with low signal while writing.
4 (2415)	Read reg VRC (Models 1-3) Envelope check (Models 4-6)	A character with incorrect parity detected in read register during write or write tape mark operation.	Indicates at least one track with low signal while writing.
5	Phase encoding	Not applicable; always set to zero.	Selected tape unit is set to PE recording mode.
6	Backward	The selected tape unit is in backward status.	Same as Models 1-3
7	C compare	C compare is a data check. It indicates that parity of data into the data register did not equal that out of the data register.	Same as Models 1-3
Note: Bits 0-4 and 7 of byte 3 indicate data checks. Any of these will set data check (bit 4, byte 0). 2415: Bit 7 causes equipment check.			
* Stop signal resulted from halt I/O instruction in CPU.			

Sense Byte 4

Bit	Designation	2401–2404, 2415 and 2420 Interpretation	
		Models 1–3 (and Models 4–6, 800 bpi, NRZI Mode)	Models 4–7 (1,600 bpi, PE)
0	Not used	Same	Same as Models 1–3
1	Reject TU	Selected tape unit failed to respond to set read or set write status when instructed, or became not ready during execution of a tape motion operation. Equipment check (bit 3, byte 0) also set.	Same as Models 1–3
2	Read clock	Maintenance aids	Not used
3	Write clock		Maintenance aid
4	Delay counter		Not used
5	C sequence	These sequence indicators are maintenance aids. They are set only in the event of a machine failure and cause equipment check and unit check. 2415: All zero bits transmitted for sense byte 4.	Set in event of a machine failure and cause a data check and unit check.
6	B sequence		
7	A sequence		

Sense Byte 5

Bit	Designation	2401–2404, 2415 and 2420 Interpretation	
		Models 1–3 (and Models 4–6, 800 bpi, NRZI Mode)	Models 4–7 (1,600 bpi, PE)
0	Reserved for future use	Always zero	Always zero
1	Reserved for CE function		
2–6	None	Always zero	Always zero
7	Reserved for RPQ use	Always zero	Always zero

After EC 730110:

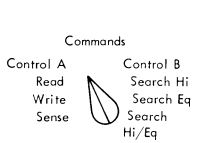
Gate 01A, Panel 2 2400 Bit 9 0729 Bit 7		P C	0	1	2 B	3 A	4 8	5 4	6 2	7 1
Designation	Card									
Read Bus	01A2	B17E	B15E	B13E	B11E	B09E	B07E	B05E	B03E	B01E
2400 Preamps	01A1	F09	F08	F07	F06	F05	F04	F03	F02	F01
Read Delay Order*										
Yellow (Forward)	01A1	C09N	C08N	C07N	C06N	C05N	C04N	C03N	C02N	C01N
Black (Backward)	01A1	C09R	C08R	C07R	C06R	C05R	C04R	C03R	C02R	C01R
Write Delay Order**	01A1	F26A	F26C	F26B	F25D	F25A	F25C	F25B	F24A	F24B
Assymmetry	01A1	D29	D28	D27	D26	D25	D24	D23	D22	D21

* Read Delay Order: C Row A, B, C, D, E, F
** Write Delay Order: G23, G24, G25, G26, ABC, D, E, F, G, H, K, L, M, N, P, Q, R

Note: Mechanical skew, seven-track, use bits P and 7.
Mechanical skew, nine-track, use bits 4 and 5.

2820 Control Unit

Channel Commands

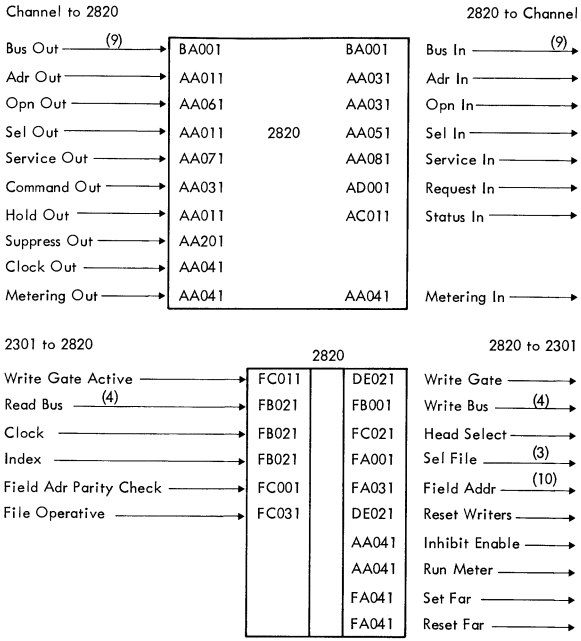


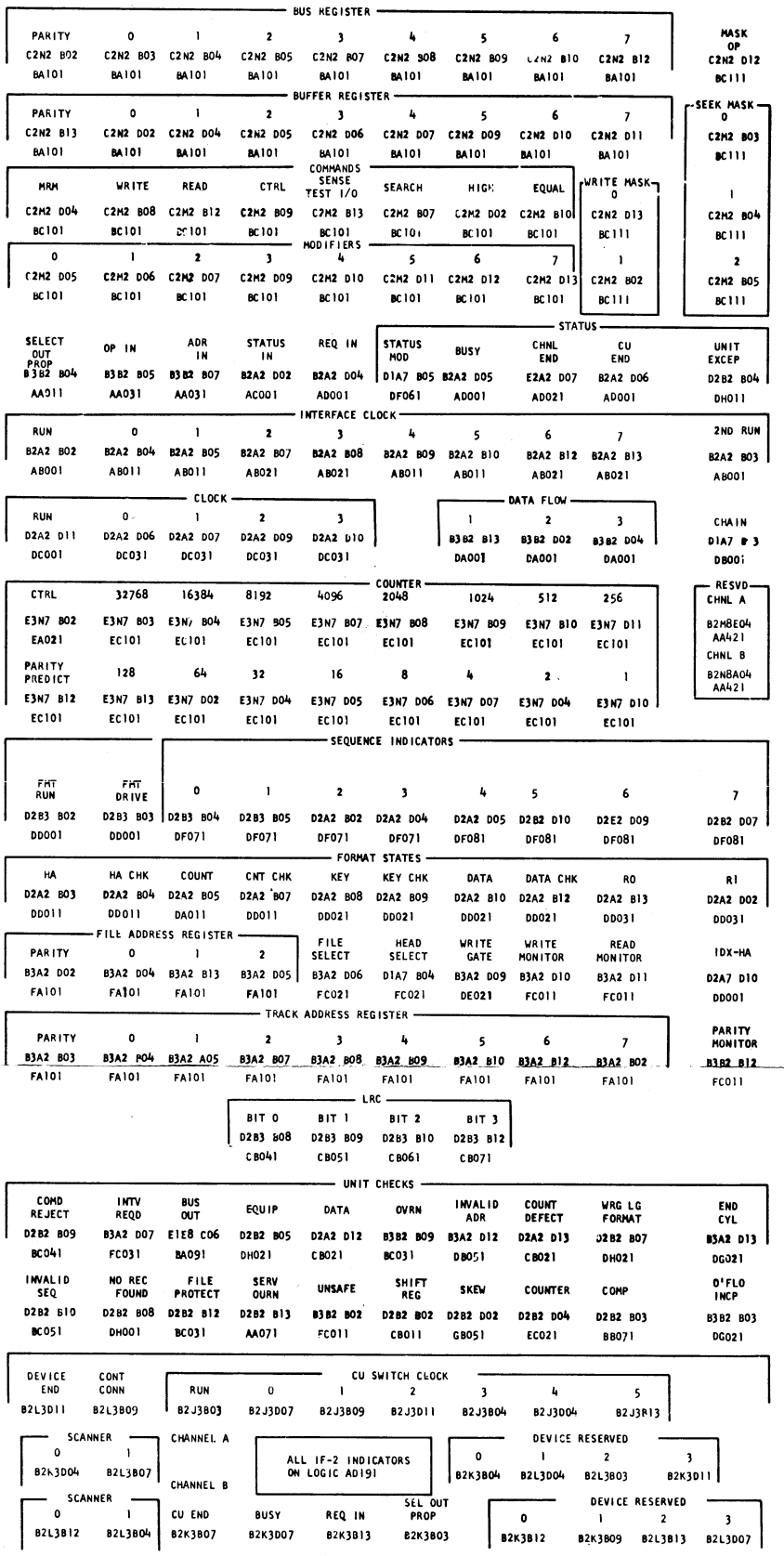
Commands	0 M/T	1 HI	2 =	Command Modifier 2^2 3 C	2^1 4 K	2^0 5 D	6 Channel	7 Channel
Write Data	0	0	0	0	0	1	0	1
Write Key, Data	0	0	0	0	1	1	0	1
Write Count, Key, Data	0	0	0	1	1	1	0	1
Write Home Address	0	0	0	1	1	0	0	1
Write Record Zero	0	0	0	1	0	1	0	1
Write Overflow	0	0	0	0	0	0	0	1
Erase	0	0	0	1	0	0	0	1
Search Equal ID	X	0	1	1	0	0	0	1
Search Equal Key	X	0	1	0	1	0	0	1
Search Equal Home Address	X	0	1	1	1	0	0	1
Search HI ID	X	1	0	1	0	0	0	1
Search HI Key	X	1	0	0	1	0	0	1
Search HI Equal ID	X	1	1	1	0	0	0	1
Search HI Equal Key	X	1	1	0	1	0	0	1
Read Data	X	0	0	0	0	1	1	0
Read Key, Data	X	0	0	0	1	1	1	0
Read Count, Key, Data	X	0	0	1	1	1	1	0
Read Home Address	X	0	0	1	1	0	1	0
Read Record Zero	X	0	0	1	0	1	1	0
Read Count	X	0	0	1	0	0	1	0
Read Initial Program Load (IPL)	0	0	0	0	0	0	1	0
Control Seek (BBCCHH) ****	0	0	0	0	0	1	1	1
Control Recalibrate **	0	0	0	1	0	0	1	1
Control Restore **	0	0	0	1	0	1	1	1
Control No Op	0	0	0	0	0	0	1	1
Control Cyl Seek (CCHH) ****	0	0	0	0	1	0	1	1
Control Head Seek (HH) *	0	0	0	1	1	0	1	1
Control Set File Mask	0	0	0	1	1	1	1	1
Release ***	1	0	0	1	0	1	0	0
Reserve ***	1	0	1	1	0	1	0	0
Test I/O	0	0	0	0	0	0	0	0
Sense I/O	0	0	0	0	0	1	0	0

Note: X on search and read commands B0 can be either 0 or 1. If 0, head switching will not take place when index point is detected. If 1, head switching will take place when index point is detected (multiple track mode).

* Head seek command has the domain seek function in 2820.
** Executed as no-op in 2820.
*** Can be tested off-line by command toggle switches only.
**** Perform same seek operation.

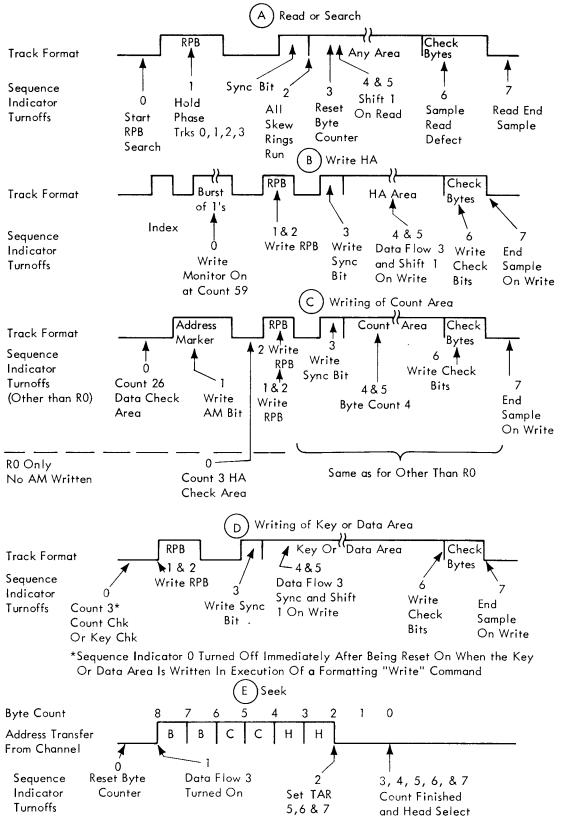
Channel Interface Lines




BUS REGISTER
PARITY 0 1 2 3 4 5 6 7
C2N2 B02 C2N2 B03 C2N2 B04 C2N2 B05 C2N2 B07 C2N2 B08 C2N2 B09 C2N2 B10 C2N2 B12
BA101 BA101 BA101 BA101 BA101 BA101 BA101 BA101 BA101
MASK OP
C2N2 D12
BC111
BUFFER REGISTER
PARITY 0 1 2 3 4 5 6 7
C2N2 B13 C2N2 D02 C2N2 D04 C2N2 D05 C2N2 D06 C2N2 D07 C2N2 D09 C2N2 D10 C2N2 D11
BA101 BA101 BA101 BA101 BA101 BA101 BA101 BA101 BA101
SEEK MASK
0 C2M2 B03 BC111
1 C2M2 B04 BC111
2 C2M2 B05 BC111
COMMANDS
MRM WRITE READ CTRL SENSE TEST I/O SEARCH HIGH EQUAL
C2M2 D04 C2M2 B08 C2M2 B12 C2M2 B09 C2M2 B13 C2M2 B07 C2M2 D02 C2M2 B10
BC101 BC101 BC101 BC101 BC101 BC101 BC101 BC101
WRITE MASK
0 C2N2 D13 BC111
1 C2M2 B02 BC111
MODIFIERS
0 1 2 3 4 5 6 7
C2M2 D05 C2M2 D06 C2M2 D07 C2M2 D09 C2M2 D10 C2M2 D11 C2M2 D12 C2M2 D13
BC101 BC101 BC101 BC101 BC101 BC101 BC101 BC101
STATUS
SELECT OUT PROP B3B2 B04 AA011
OP IN B3B2 B05 AA031
ADR IN B3B2 B07 AA031
STATUS IN B2A2 D02 AC001
REQ IN B2A2 D04 AD001
STATUS MOD D1A7 B05 DF061
BUSY B2A2 D05 AD001
CHNL END E2A2 D07 AD021
CU END B2A2 D06 AD001
UNIT EXCEP D2B2 B04 DH011
INTERFACE CLOCK
RUN 0 1 2 3 4 5 6 7 2ND RUN
B2A2 B02 B2A2 B04 B2A2 B05 B2A2 B07 B2A2 B08 B2A2 B09 B2A2 B10 B2A2 B12 B2A2 B13 B2A2 B03
AB001 AB011 AB011 AB021 AB021 AB011 AB011 AB021 AB021 AB001
CLOCK
RUN 0 1 2 3
D2A2 D11 D2A2 D06 D2A2 D07 D2A2 D09 D2A2 D10
DC001 DC031 DC031 DC031 DC031
DATA FLOW
1 2 3
B3B2 B13 B3B2 D02 B3B2 D04
DA001 DA001 DA001
CHAIN
D1A7 B 3
DB001
COUNTER
CTRL 32768 16384 8192 4096 2048 1024 512 256
E3N7 B02 E3N7 B03 E3N7 B04 E3N7 B05 E3N7 B07 E3N7 B08 E3N7 B09 E3N7 B10 E3N7 D11
EA021 EC101 EC101 EC101 EC101 EC101 EC101 EC101 EC101
PARITY PREDICT 128 64 32 16 8 4 2 1
E3N7 B12 E3N7 B13 E3N7 D02 E3N7 D04 E3N7 D05 E3N7 D06 E3N7 D07 E3N7 D04 E3N7 D10
EC101 EC101 EC101 EC101 EC101 EC101 EC101 EC101 EC101
RESVD
CHNL A
B2N8E04 AA421
CHNL B
B2N8A04 AA421
SEQUENCE INDICATORS
FMT RUN D2B3 B02 DD001
FMT DRIVE D2B3 B03 DD001
0 D2B3 B04 DF071
1 D2B3 B05 DF071
2 D2A2 B02 DF071
3 D2A2 D04 DF071
4 D2A2 D05 DF081
5 D2B2 D10 DF081
6 D2E2 D09 DF081
7 D2B2 D07 DF081
FORMAT STATES
HA D2A2 B03 DD011
HA CHK D2A2 B04 DD011
COUNT D2A2 B05 DA011
CNT CHK D2A2 B07 DD011
KEY D2A2 B08 DD021
KEY CHK D2A2 B09 DD021
DATA D2A2 B10 DD021
DATA CHK D2A2 B12 DD021
RO D2A2 B13 DD031
RI D2A2 D02 DD031
FILE ADDRESS REGISTER
PARITY B3A2 D02 FA101
0 B3A2 D04 FA101
1 B3A2 B13 FA101
2 B3A2 D05 FA101
FILE SELECT B3A2 D06 FC021
HEAD SELECT D1A7 B04 FC021
WRITE GATE B3A2 D09 DE021
WRITE MONITOR B3A2 D10 FC011
READ MONITOR B3A2 D11 FC011
IDX-HA D2A7 D10 DD001
TRACK ADDRESS REGISTER
PARITY B3A2 B03 FA101
0 B3A2 P04 FA101
1 B3A2 A05 FA101
2 B3A2 B07 FA101
3 B3A2 B08 FA101
4 B3A2 B09 FA101
5 B3A2 B10 FA101
6 B3A2 B12 FA101
7 B3A2 B02 FA101
PARITY MONITOR B3B2 B12 FC011
LRC
BIT 0 D2B3 B08 CB041
BIT 1 D2B3 B09 CB051
BIT 2 D2B3 B10 CB061
BIT 3 D2B3 B12 CB071
UNIT CHECKS
COMD REJECT D2B2 B09 BC041
INTV REQD B3A2 D07 FC031
BUS OUT E1E8 C06 BA091
EQUIP D2B2 B05 DH021
DATA D2A2 D12 CB021
OVRN B3B2 B09 BC031
INVALID ADR B3A2 D12 DB051
COUNT DEFECT D2A2 D13 CB021
WRG LG FORMAT D2B2 B07 DH021
END CYL B3A2 D13 DG021
INVALID SEQ D2B2 B10 BC051
NO REC FOUND D2B2 B08 DH001
FILE PROTECT D2B2 B12 BC031
SERV OURN D2B2 B13 AA071
UNSAFE B3B2 B02 FC011
SHIFT REG D2B2 B02 CB011
SKEW D2B2 D02 GB051
COUNTER D2B2 D04 EC021
COMP D2B2 B03 BB071
O'FLO INCP B3B2 B03 DG021
DEVICE END B2L3D11
CONT CONN B2L3B09
CU SWITCH CLOCK
RUN B2J3B03
0 B2J3D07
1 B2J3B09
2 B2J3D11
3 B2J3B04
4 B2J3D04
5 B2J3R13
SCANNER
0 B2K3D04
1 B2L3B07
CHANNEL A
CHANNEL B
ALL IF-2 INDICATORS ON LOGIC AD191
DEVICE RESERVED
0 B2K3B04
1 B2L3D04
2 B2L3B03
3 B2K3D11
SCANNER
0 B2L3B12
1 B2L3B04
CU END B2K3B07
BUSY B2K3D07
REQ IN B2K3B13
SEL OUT PROP B2K3B03
DEVICE RESERVED
0 B2K3B12
1 B2K3B09
2 B2L3B13
3 B2L3D07

2820 Control Unit (Continued)

Sequence Indicators



2820 Control Unit (Continued)

Sense Byte Definition

BYTE 0		COMMENTS
Bit 0	Command Reject	
1	Intervention Required	
2	Bus Out Check	
3	Equipment Check	
4	Data Check	
5	Overrun	Set by late command or service overrun
6		Not used
7	Invalid Address	Command reject is also set

BYTE 1		
Bit 0	Data Check in Count Field	Data check is also set
1	Track Overrun	
2	End of Cylinder	
3	Invalid Sequence	Command reject is also set
4	No Record Found	
5	File Protect	Command reject may also be set
6	Service Overrun	Overrun is also set
7	Overflow Incomplete	File protect or end of cylinder or invalid sequence; command reject may also be set.

BYTE 2		
Bit 0	Unsafe	Equipment check is also set
1	Shift Register Check	Equipment check is also set
2	Skew Failure	Equipment check and LRC bit(s) also set
3	Counter Check	Equipment check is also set
4	Compare Check	Equipment check is also set
5		Not used
6		Not used
7		Not used

BYTE 3		
Bit 0	Longitudinal	Drum bit 0 parity error
1	Redundancy	Drum bit 1 parity error
2	Checks	Drum bit 2 parity error
3		Drum bit 3 parity error (Data check or skew failure is also set with drum bit parity error.)
4–7		Not used

BYTE 4		
Bit 0	Sequence Indicator 0	
1	Sequence Indicator 1	
2	Sequence Indicator 2	If any sequence indicator is on when sampled, equipment check is set.
3	Sequence Indicator 3	
4	Sequence Indicator 4	
5	Sequence Indicator 5	
6	Sequence Indicator 6	
7	Sequence Indicator 7	

2820 Control Unit (Continued)

Sense Byte Definition (Continued)

BYTE 5	COMMENTS
Bit 0-4	Not used--all zeros
5	Data modifier 1
6	Read operation
7	Write operation
	Overflow incomplete is also set

Byte 5 contains a command byte which informs the channel whether an overflow incomplete occurred on a read data or a write data operation. All sense bits in bytes 0, 1, 2, and 3 cause unit check to appear in the status byte.

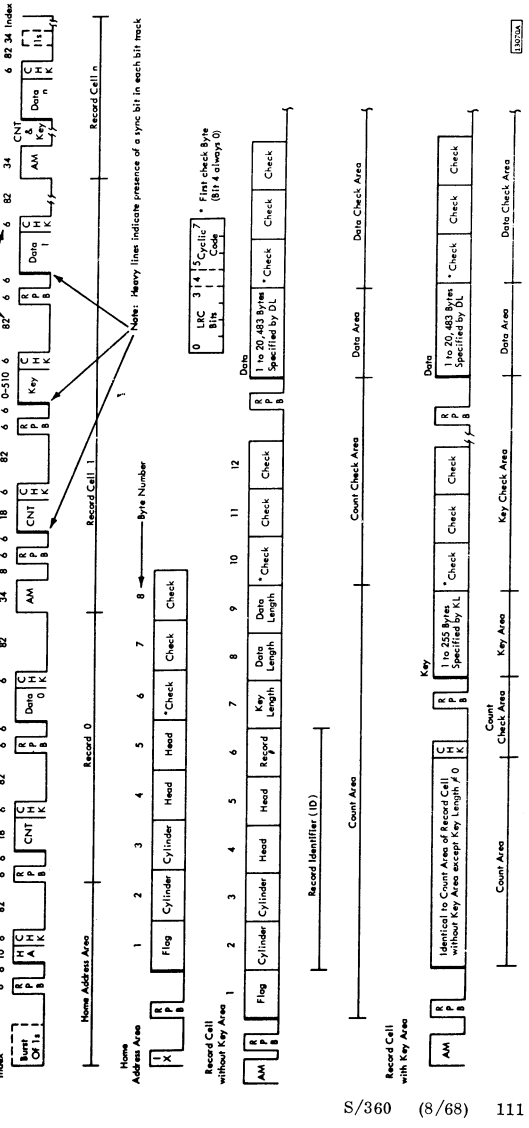
File Mask Register

Write Mask		Seek Mask			Always Zero		
B0	B1	B2	B3	B4	B5	B6	B7

Write Mask		Significance
B0	B1	
1	1	Permit all write commands
0	0	Permit all write commands except write home address and write R0
1	0	Permit all write commands except write HA, R0, CKD, CKD erase and CKD overflow
0	1	Permit no write commands

Seek Mask			Significance
B2	B3	B4	
0	0	0	Permit all seek commands
0	0	1	Permit cylinder seek and head seek
0	1	0	Permit head seek
0	1	1	Permit no seek commands
1	0	0	Invalid
1	0	1	Invalid
1	1	0	Invalid
1	1	1	Invalid

2301 Track Format



2301 Head Conversion

			Section 0		Section 1		Section 2		Section 3		Section 4	
		2301 Head Reg	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex	Dec	Hex
Upper Racks	00	00	0	00	40	28	80	50	120	78	160	A0
	01	01	1	01	41	29	81	51	121	79	161	A1
	02	02	2	02	42	2A	82	52	122	7A	162	A2
	03	03	3	03	43	2B	83	53	123	7B	163	A3
	04	04	4	04	44	2C	84	54	124	7C	164	A4
	05	05	5	05	45	2D	85	55	125	7D	165	A5
	06	06	6	06	46	2E	86	56	126	7E	166	A6
	07	07	7	07	47	2F	87	57	127	7F	167	A7
	08	08	8	08	48	30	88	58	128	80	168	A8
	09	09	9	09	49	31	89	59	129	81	169	A9
	10	10	10	0A	50	32	90	5A	130	82	170	AA
	11	11	11	0B	51	33	91	5B	131	83	171	AB
	12	12	12	0C	52	34	92	5C	132	84	172	AC
	13	13	13	0D	53	35	93	5D	133	85	173	AD
	14	14	14	0E	54	36	94	5E	134	86	174	AE
	15	15	15	0F	55	37	95	5F	135	87	175	AF
	16	16	16	10	56	38	96	60	136	88	176	B0
	17	17	17	11	57	39	97	61	137	89	177	B1
	18	18	18	12	58	3A	98	62	138	8A	178	B2
	19	19	19	13	59	3B	99	63	139	8B	179	B3
Lower Racks	00	20	20	14	60	3C	100	64	140	8C	180	B4
	01	21	21	15	61	3D	101	65	141	8D	181	B5
	02	22	22	16	62	3E	102	66	142	8E	182	B6
	03	23	23	17	63	3F	103	67	143	8F	183	B7
	04	24	24	18	64	40	104	68	144	90	184	B8
	05	25	25	19	65	41	105	69	145	91	185	B9
	06	26	26	1A	66	42	106	6A	146	92	186	BA
	07	27	27	1B	67	43	107	6B	147	93	187	BB
	08	28	28	1C	68	44	108	6C	148	94	188	BC
	09	29	29	1D	69	45	109	6D	149	95	189	BD
	10	30	30	1E	70	46	110	6E	150	96	190	BE
	11	31	31	1F	71	47	111	6F	151	97	191	BF
	12	32	32	20	72	48	112	70	152	98	192	C0
	13	33	33	21	73	49	113	71	153	99	193	C1
	14	34	34	22	74	4A	114	72	154	9A	194	C2
	15	35	35	23	75	4B	115	73	155	9B	195	C3
	16	36	36	24	76	4C	116	74	156	9C	196	C4
	17	37	37	25	77	4D	117	75	157	9D	197	C5
	18	38	38	26	78	4E	118	76	158	9E	198	C6
	19	39	39	27	79	4F	119	77	159	9F	199	C7

Reader Commands

	Bit 0	1	2	3	4	5	6	7
Read	X	X	X	0	0	0	1	0
Control	X	X	X	0	0	0	1	1
Sense	0	0	0	0	0	1	0	0
*Write Diagnostic	0	0	1	0	0	1	0	1
Check Read	1	1	0	0	0	1	1	0
1400 Compat Read	1	1	0	1	0	0	1	0
No-Op	0	0	0	0	0	0	1	1

Modifier Bit 0	1	2	
X	X	0	Read (Data Mode 1)
X	X	1	Read (Data Mode 2)
0	0	X	Read and Feed – Stacker Select R1
0	1	X	Read and Feed – Stacker Select R2
1	0	X	Read and Feed – Stacker Select RP3
1	1	X	Read–No Feed
0	0	1	Feed Stacker Select R1 (Control)
0	1	1	Feed Stacker Select R2 (Control)
1	0	1	Feed Stacker Select RP3 (Control)

Punch Commands

	Bit 0	1	2	3	4	5	6	7
Write and SS	X	X	X	0	0	0	0	1
Read	1	1	0	0	0	0	1	0
Sense	0	0	0	0	0	1	0	0
No-Op	0	0	0	0	0	0	1	1
1400 Compatibility Write	X	X	X	1	0	0	0	1
PFR Write Feed and SS	X	X	X	0	1	0	0	1
1400 Compatibility PFR Write Feed and SS	X	X	X	1	1	0	0	1
Diagnostic Check Read	1	1	0	0	0	1	1	0

Modifier Bit 0	1	2	
X	X	0	Write (Data Mode 1)
X	X	1	Write (Data Mode 2)
0	0	X	Write Feed and Stacker Select P1
0	1	X	Write Feed and Stacker Select P2
1	0	X	Write Feed and Stacker Select RP3

*This command is addressed to the punch.

Printer Commands

	Bit 0	1	2	3	4	5	6	7
Write	X	X	X	X	X	0	0	1
Control (Space - Skip)	X	X	X	X	X	0	1	1
Write and Space Suppress	0	0	0	0	0	0	0	1
No-Op	0	0	0	0	0	0	1	1
Diagnostic Read	0	0	0	0	0	0	1	0
Print Check Read	0	0	0	0	0	1	1	0
Diagnostic Write	0	0	0	0	0	1	0	1
Sense	0	0	0	0	0	1	0	0

Modifier Bit 0 1 2 3 4	
0 0 0 0 1	Space 1
0 0 0 1 0	Space 2
0 0 0 1 1	Space 3
1 0 0 0 1	Skip to Channel 1
1 0 0 1 0	Skip to Channel 2
1 1 1 0 0	Skip to Channel 12

UCB Only

	Bit 0	1	2	3	4	5	6	7
Block Data	0	1	1	1	0	0	1	1
Reset Block Data Check	0	1	1	1	1	0	1	1
Condition Load Format	1	1	1	0	1	0	1	1
Load UCB Folding	1	1	1	1	0	0	1	1
Load UCB No Folding	1	1	1	1	1	0	1	1

1404 Printer

Feed and Write	X	X	X	X	X	1	0	1
Read	0	0	0	0	0	0	1	0
Diagnostic Check Read	0	0	0	0	0	1	1	0

Reader/Punch Status Bits

Bit	Name	Description
0	Attention	Used only in 1400 compatibility mode. The bit is on only during the 6.5 milliseconds that the 1400 provisional feed latch is active. It indicates the time when a valid stacker select command can be given to the reader. Logic 42.14.01.1.
1		Not Used.
2		Not Used.
3	Busy	The device is executing a previous command, or a device-end or channel-end is pending.
4	Channel End	Signifies the end of data transfer. This bit will not be set by a rejected control command.
5	Device End	Signifies completion of the previous command or the device has just been made ready. This bit is not set by test I/O or a rejected command.
6	Unit Check	Unit check is set by the errors and interlocks stored in sense register bits 0, 1, 2, 3, 4, and 6.
7	Unit Exception	Unit exception or end-of-file pertains to the reader and PFR. The reader has processed and stacked the last card. 'Ready' is not allowed to drop until unit exception has been presented to the channel. When unit exception is signaled for a PFR read command, a card is still at the pre-check station.

Printer Status Bits

Bit	Name	Description
0		Not Used.
1		Not Used.
2		Not Used.
3	Busy	The printer is executing a previous command, or a device-end status is pending.
4	Channel End	Signifies the end of the printer's use of the channel. This bit is not set by a test I/O command or if a command is rejected during initial selection.
5	Device End	Signifies completion of the previous command, or the printer has just been made ready. This bit is not set by test I/O or a rejected command.
6	Unit Check	Unit check is an indication of the various errors and interlocks stored in the sense register.
7	Unit Exception	Unit exception indicates channel 12 has been sensed in the carriage tape.

Sense Byte, Reader

0	Command Reject	A command has been received that is unacceptable to the reader, such as 'write' or 'read backward'. Two consecutive feeds with no intervening read is also rejected.
1	Intervention Required	'Ready' has dropped due to: Stacker full — Transport jam Hopper empty — Stop key Feed stop — Cover open
2	Bus-Out Parity Check	Bus-out parity check of the command.
3	Equipment Check	A card reader error: Translate check Address check Hole count Data register parity.
4	Data Check	Invalid card code was read. More than one hole punched in rows 1-7 in any one column.

Sense Byte, Reader (Continued)

Bit	Name	Description
5		Not Used.
6	Unusual Command	Two successive read commands without an intervening feed.
7		Not Used.

Sense Byte, Punch

0	Command Reject	A command was received that is not acceptable to the punch, such as 'read backward' or 'control'. (In PFR mode, two successive PFR write commands without an intervening punch-read command are also rejected.)
1	Intervention Required	The punch is not ready due to: Stop key — Stacker full Hopper empty — Feed stop Chip box full or missing — Transport jam Cover switch.
2	Bus-Out Parity Check	Bus-out parity check of the command or data being transferred. (Note: Card will not be punched.)
3	Equipment Check	A punch error from: Punch translate — Data register parity Hole-count check — Address check
4	Data Check	(Used only with optional punch feed read feature.) An invalid card code was read. More than one punch in rows 1-7 in any one column.
5		Not Used.
6	Unusual Command	(Used only with optional punch feed read feature.) Two successive read commands were received.
7		Not Used.

Sense Byte, Printer

Bit	Name	Description
0	Command Reject	A command was received that cannot be executed, such as 'read backward' or 'space' more than three lines. If the UCB feature is installed, a load UCB command will be rejected if it is not preceded by a condition load format command.
1	Intervention Required	'Ready' has dropped due to: 'End of forms' or 'forms check' Stop key pressed Sync check Mechanical interlock open
2	Bus-Out Check	Bus-out parity of the command or data being transferred.
3	Equipment Check	This is a program-resettable error. A print buffer parity check or hammer check was detected.
4	Data Check	Indicates an 'uncomparable character' was detected (UCS only). If a 1404 is attached, it indicates an invalid card code was detected with the read compare feature. (Note: An invalid card code is defined as having two or more punches in rows 1-7 in any given column.)
5	UCS Parity	A parity error was detected in the UCS buffer (UCS only).
6	Unusual Command Sequence	1404 only.
7	Channel 9	Channel 9 was sensed by the carriage brushes.

2821 Print Hammer Driver Locations

Print Position	Location	Print Position	Location	Print Position	Location
01	G-25	45	G-14	89	G-10
02	G-25	46	E-14	90	G-10
03	E-18	47	E-14	91	G-21
04	E-18	48	G-14	92	G-21
05	G-18	49	G-14	93	E-09
06	E-18	50	G-14	94	E-09
07	E-18	51	G-23	95	G-09
08	G-18	52	G-23	96	E-09
09	G-18	53	E-13	97	E-09
10	G-18	54	E-13	98	G-09
11	G-25	55	G-13	99	G-09
12	G-25	56	E-13	100	G-09
13	E-17	57	E-13	101	G-20
14	E-17	58	G-13	102	G-20
15	G-17	59	G-13	103	E-08
16	E-17	60	G-13	104	E-08
17	E-17	61	G-22	105	G-08
18	G-17	62	G-22	106	E-08
19	G-17	63	E-12	107	E-08
20	G-17	64	E-12	108	G-08
21	G-24	65	G-12	109	G-08
22	G-24	66	E-12	110	G-08
23	E-16	67	E-12	111	G-20
24	E-16	68	G-12	112	G-20
25	G-16	69	G-12	113	E-07
26	E-16	70	G-12	114	E-07
27	E-16	71	G-22	115	G-07
28	G-16	72	G-22	116	E-07
29	G-16	73	E-11	117	E-07
30	G-16	74	E-11	118	G-07
31	G-24	75	G-11	119	G-07
32	G-24	76	E-11	120	G-07
33	E-15	77	E-11	121	G-19
34	E-15	78	G-11	122	G-19
35	G-15	79	G-11	123	E-06
36	E-15	80	G-11	124	E-06
37	E-15	81	G-21	125	G-06
38	G-15	82	G-21	126	E-06
39	G-15	83	E-10	127	E-06
40	G-15	84	E-10	128	G-06
41	G-23	85	G-10	129	G-06
42	G-23	86	E-10	130	G-06
43	E-14	87	E-10	131	G-19
44	E-14	88	G-10	132	G-19

Commands

Command Type	Command Name	Hex Code	
		Single Track	Multi-Track
Control	Seek (BB CC HH)	07	--
	Seek Cylinder (CC HH)	0B	--
	Seek Head (HH)	1B	--
	Recalibrate	13	--
	No Operation	03	--
	Set File Mask	1F	--
	Space Count	0F	--
	Restore (2321 only)	17	--
Sense	Test I/O	00	--
	Sense I/O	04	--
Read	Read Data	06	86
	Read Key-Data	0E	8E
	Read-Count-Key-Data	1E	9E
	Read Home Address	1A	9A
	Read R0	16	96
	Read Count	12	92
	Read IPL	02	--
Write	Write Data	05	--
	Write Key-Data	0D	--
	Write-Count-Key-Data	1D	--
	Write Home Address	19	--
	Write R0	15	--
	** Write (Special) Count-Key-Data	01	--
	Erase	11	--
Search	Search Equal ID	31	B1
	Search High ID	51	D1
	Search Equal-Hi-ID	71	F1
	Search Equal Key	29	A9
	Search High Key	49	C9
	Search Equal-Hi Key	69	E9
	Search Equal HA	39	B9
	*** Search Equal Key Data	2D	AD
	*** Search High Key Data	4D	CD
	*** Search Hi-Eq Key Data	6D	ED
	**** Continue Scan Equal	25	A5
	**** Continue Scan High	45	C5
	**** Continue Scan Hi Eq	65	E5
	**** Continue Scan, No Compare	55	D5
	**** Continue Scan, Set Compare	75, 35	F5, B5
Switching	* Reserve Device	B4	--
	* Release Device	94	--
MSC †	Initiate Buffer	E3	
	Load Buffer	E1	
	Read Buffer	E2	
	Buffer Reset	C3	

* Special feature used with Two-Channel Switch.
** Special feature used with Record Overflow.
*** Special feature used with File Scan.
**** Used with File Scan with Record Overflow.
† MSC 2314 Multiplex Storage Control Feature (RPQ).

Seek Address

Type	Cell Number		Cylinder Number		Head Number	
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
2311	0	0	0	0-202	0	0-9
2302 Models 3 and 4	0	0	0	0-249	0	0-45
2303	0	0	0	0-79	0	0-9
2321	0	0-9	0-19	0-9	0-4	0-19
			Subcell	Strip	Bar	Head No.
2314	0	0	0	0-202	0	0-19

File Protection

The significance of the file mask bits is:

B0	B1	
0	0	Inhibit Write Home Address and Write R0
0	1	Inhibit all write commands
1	0	Inhibit Write Home Address - Inhibit Write R0 - Inhibit Write Count, Key, and Data
1	1	Permit all write commands

B3	B4	
0	0	Permit all seek and restore commands
0	1	Permit Seek CCHH and HH CCWs
1	0	Permit Seek HH CCW
1	1	Inhibit all seek commands

B2	B5	B6	B7
0	0	0	0

Status Byte

Bit	Name	Note
0	Attention	Not Used
1	Status Modifier	Used with Search and Control Unit Busy.
2	Control Unit End	The control unit has finished an operation.
3	Busy	Indicates addressed access mechanism is moving; or used in conjunction with Status Modifier to indicate Control Unit Busy.
4	Channel End	The control unit has received all the data from the channel needed to do the operation called for and the channel is freed.
5	Device End	Indicates that an access mechanism is free to be used.
6	Unit Check	Indicates that a control unit or programming error or device hardware check has been detected.
7	Unit Exception	End-of-File.

Sense Information Summary

Sense Bit: Position	Condition
Byte 0 Bit	
0	Command Reject includes Invalid Command, Invalid Sequence, and File Protected.
1	Intervention Required
2	Bus Out Parity
3	Equipment Check
4	Data Check
5	Overrun
6	Track Condition Check
7	Seek Check
Byte 1 Bit	
0	Data check in count field; also causes Byte 0, Bit 4 (Data Check) to be turned on.
1	Track Overrun. Indicated on Write.
2	End of Cylinder
3	Invalid Sequence also causes Command Reject (Byte 0, Bit 0) to be turned on.
4	No Record Found
5	File Protected also causes Command Reject (Byte 0, Bit 0)
6	Missing Address Marker
7	Overflow Incomplete
Byte 2 Bit	
0	Unsafe
1	Not Used
2	Serializer/Deserializer Check — Also turn on Equipment Check Byte 0, Bit 3
3	Not Used
4	ALU Check
5	Unselected Status

Byte 3

Bit	2311	2321	2302	2303	2314
0	Ready	Drive Ready	Access Ready		Busy
1	On Line	Drive Operative	Access Operative		On Line
2	Unsafe	Read Safety	Read Safety		Unsafe
3	----------	Write Safety	Write Safety		Not Used
4	On Line	Strip Ready	On Line	On Line	Pack Change
5	End of Cylinder	Invalid Address	----------		End of Cylinder
6	----------	Auto Restore	----------		Not Used
7	Seek Incomplete	CE Cell Located	CE Cylinder Located		Seek Incomplete

Sense Information Summary (Continued)

Sense Bit Position	Condition
Byte 4 (2314 Only)	
Bit	
0	Wrong Length Record. Multiplex Storage Control Feature.
1	Pending Status. Multiplex Storage Control Feature.
2-3	Not Used
4-7	Module Identification. Because each of the nine physical disk modules may be assigned any of the eight logical drive (or module) addresses, means is provided to allow the system program to identify which particular module is assigned a given address. Sense byte 4 contains the identity of the physical drive corresponding to the address to which the sense command was issued, according to the following code:

Sense Byte 4 Bits 01234567	Physical Drive
xx000000	A
xx000001	B
xx000010	C
xx000011	D
xx000100	E
xx000101	F
xx000110	G
xx000111	H
xx001000	J
xx001111	Module not Defined

Note: Bits 0 and 1 (xx) are used in the Multiplex Storage Control Feature (RPQ S50001).

Byte 5

This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). When overflow incomplete occurs, this byte has one of the following configurations:

00000110 - A read command was in progress when the overflow incomplete interrupt occurred.

00000101 - A non-formating write command was in progress.

00100101 - A search equal key data command was in progress, and the compare is equal to this point.

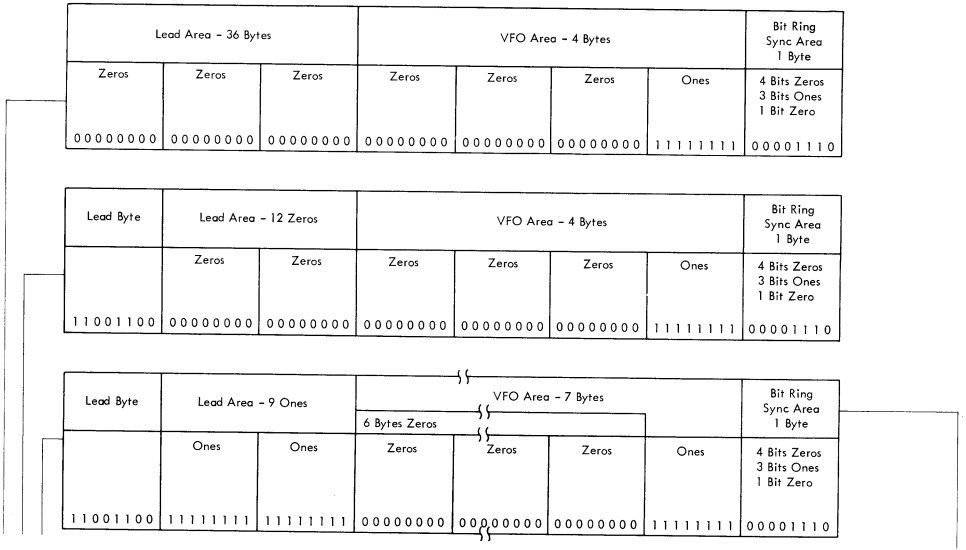
01000101 - A search high key data command was in progress, and the compare is equal to this point.

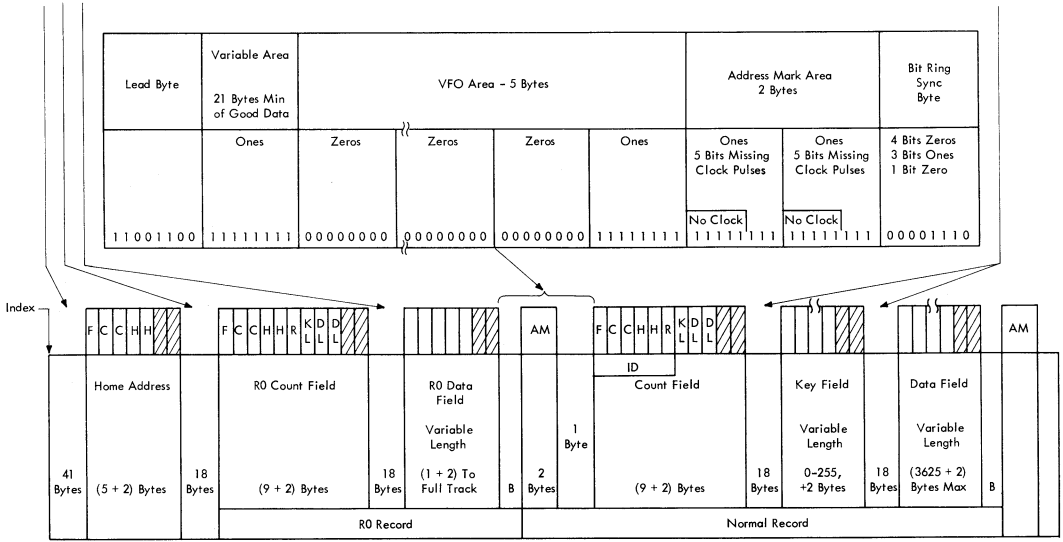
01100101 - A search high or equal key data command was in progress, and the compare is equal to this point.

01010101 - Any search key data was in progress and the compare is low, or a search equal key data was in progress and the compare is unequal to this point (i. e., it has already been determined that no status modifier would be set on the entire logical record.)

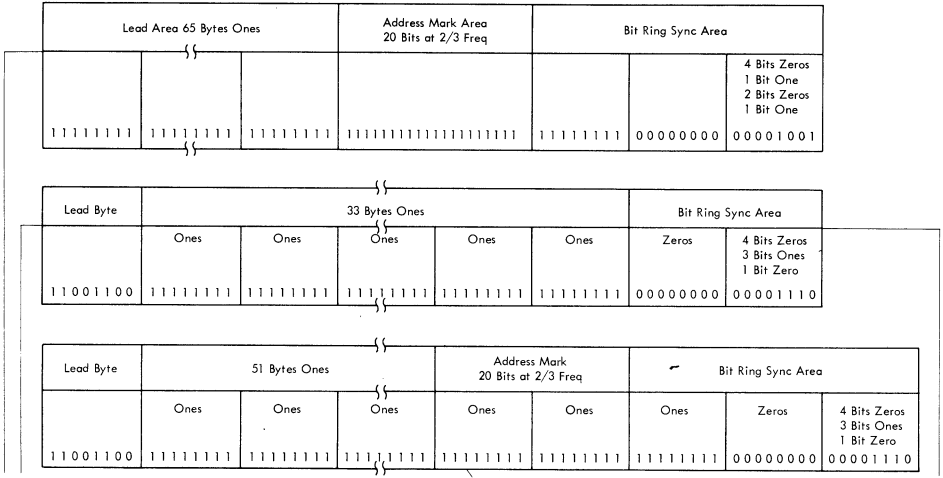
01110101 - A search high or high-equal key data command was in progress, and the compare is high to this point (i.e., it has already been determined that a status modifier would be set on the logical record).

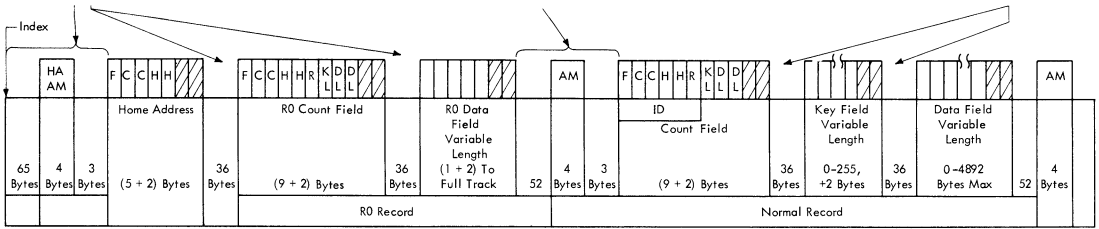
Data Format (2302)




Lead Byte
Variable Area
21 Bytes Min of Good Data
VFO Area - 5 Bytes
Address Mark Area 2 Bytes
Bit Ring Sync Byte
Ones
Zeros
Zeros
Zeros
Ones
Ones 5 Bits Missing Clock Pulses
Ones 5 Bits Missing Clock Pulses
4 Bits Zeros 3 Bits Ones 1 Bit Zero
No Clock
No Clock
11001100
11111111
00000000
00000000
00000000
11111111
11111111
11111111
00001110
Index
F C C H H R K L D L D L
AM
ID
Home Address
R0 Count Field
R0 Data Field
Variable Length
1 Byte
Count Field
Key Field
Variable Length
Data Field
Variable Length
41 Bytes
(5 + 2) Bytes
18 Bytes
(9 + 2) Bytes
18 Bytes
(1 + 2) To Full Track
B
2 Bytes
(9 + 2) Bytes
18 Bytes
0-255, +2 Bytes
18 Bytes
(3625 + 2) Bytes Max
B
R0 Record
Normal Record

Data Format (2303)



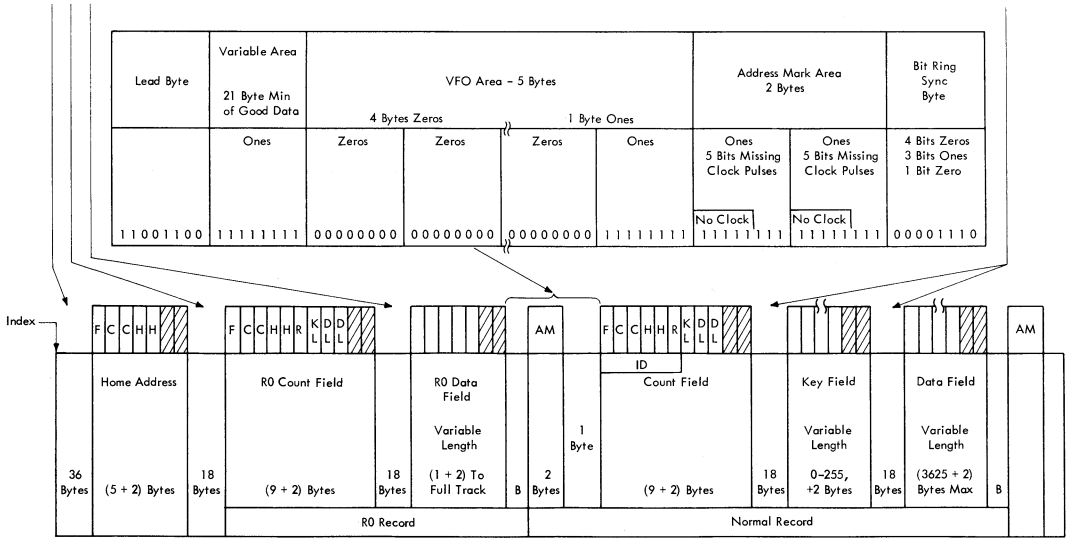

Index
HA
AM
F C C H H
Home Address
F C C H H R K D D
L L L
R0 Count Field
R0 Data
Field
Variable
Length
(1 + 2) To
Full Track
AM
F C C H H R K D D
L L L
ID
Count Field
Key Field
Variable
Length
Data Field
Variable
Length
AM
65
Bytes
4
Bytes
3
Bytes
(5 + 2) Bytes
36
Bytes
(9 + 2) Bytes
36
Bytes
52
Bytes
4
Bytes
3
Bytes
(9 + 2) Bytes
36
Bytes
0-255,
+2 Bytes
36
Bytes
0-4892
Bytes Max
52
Bytes
4
Bytes
R0 Record
Normal Record

Data Format (2311)

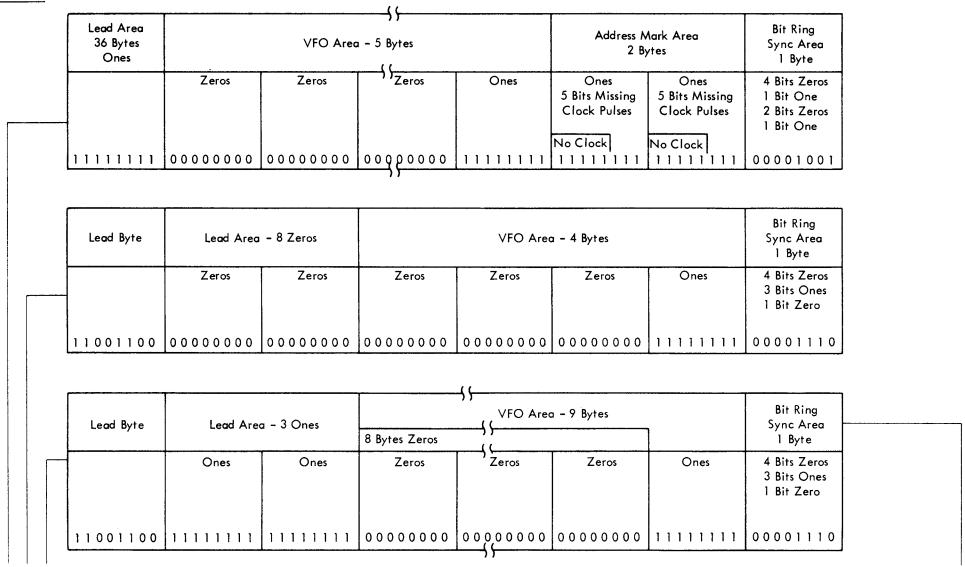
Lead Area - 31 Bytes			VFO Area - 4 Bytes				Bit Ring Sync Area 1 Byte
Zeros	Zeros	Zeros	Zeros	Zeros	Zeros	Ones	4 Bits Zeros 3 Bits Ones 1 Bit Zero
00000000	00000000	00000000	00000000	00000000	00000000	11111111	00001110

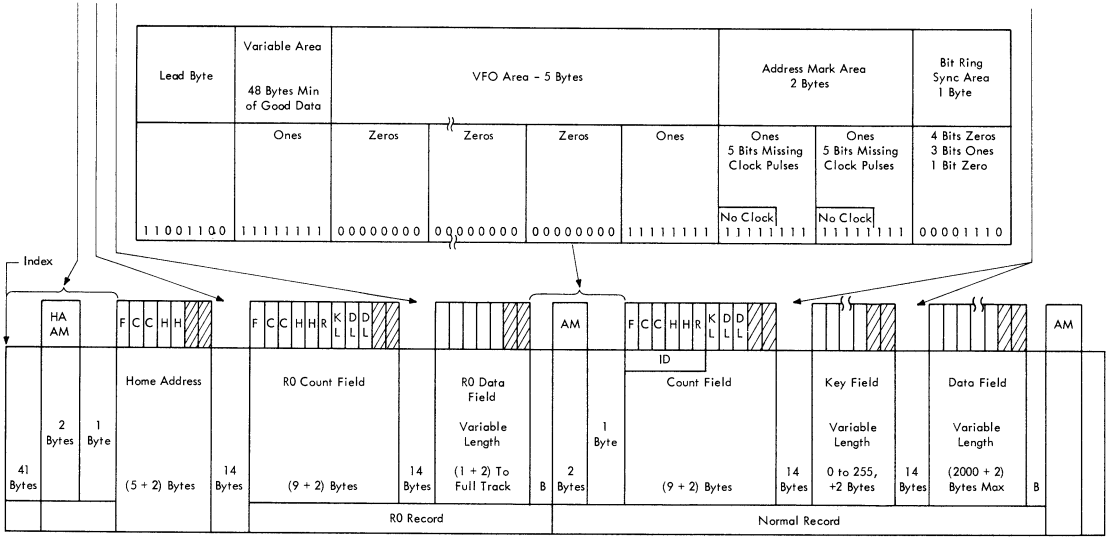
Lead Byte	Lead Area - 12 Zeros		VFO Area - 4 Bytes				Bit Ring Sync Area 1 Byte
	Zeros	Zeros	Zeros	Zeros	Zeros	Ones	4 Bits Zeros 3 Bits Ones 1 Bit Zero
11001100	00000000	00000000	00000000	00000000	00000000	11111111	00001110

Lead Byte	Lead Area - 9 Ones		VFO Area - 7 Bytes				Bit Ring Sync Area 1 Byte
			6 Bytes Zeros				
	Ones	Ones	Zeros	Zeros	Zeros	Ones	4 Bits Zeros 3 Bits Ones 1 Bit Zero
11001100	11111111	11111111	00000000	00000000	00000000	11111111	00001110

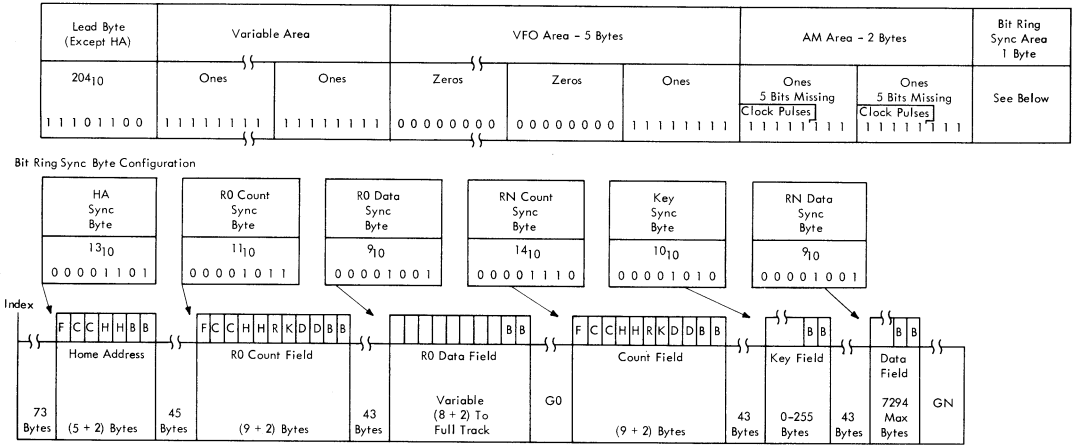

Lead Byte
Variable Area
21 Byte Min of Good Data
VFO Area – 5 Bytes
4 Bytes Zeros
1 Byte Ones
Address Mark Area 2 Bytes
Bit Ring Sync Byte
Ones
Zeros
Zeros
Zeros
Ones
Ones 5 Bits Missing Clock Pulses
Ones 5 Bits Missing Clock Pulses
4 Bits Zeros 3 Bits Ones 1 Bit Zero
11001100
11111111
00000000
00000000
00000000
11111111
No Clock
11111111
No Clock
11111111
00001110
Index
F C C H H
F C C H H R K D D L L
AM
F C C H H R K D D L L
ID
AM
Home Address
R0 Count Field
R0 Data Field
Variable Length
1 Byte
Count Field
Key Field
Variable Length
Data Field
Variable Length
36 Bytes
(5 + 2) Bytes
18 Bytes
(9 + 2) Bytes
18 Bytes
(1 + 2) To Full Track
B
2 Bytes
(9 + 2) Bytes
18 Bytes
0–255, +2 Bytes
18 Bytes
(3625 + 2) Bytes Max
B
R0 Record
Normal Record

Data Format (2321)




Lead Byte
Variable Area
48 Bytes Min of Good Data
VFO Area – 5 Bytes
Address Mark Area 2 Bytes
Bit Ring Sync Area 1 Byte
Ones
Zeros
Zeros
Zeros
Ones
Ones 5 Bits Missing Clock Pulses
Ones 5 Bits Missing Clock Pulses
4 Bits Zeros 3 Bits Ones 1 Bit Zero
11001100
11111111
00000000
00000000
00000000
11111111
No Clock
11111111
No Clock
11111111
00001110
Index
HA AM
F C C H H R K L D D L L
AM
ID
Home Address
R0 Count Field
R0 Data Field
Variable Length
Count Field
Key Field
Variable Length
Data Field
Variable Length
41 Bytes
2 Bytes
1 Byte
(5 + 2) Bytes
14 Bytes
(9 + 2) Bytes
14 Bytes
(1 + 2) To Full Track
B
2 Bytes
1 Byte
(9 + 2) Bytes
14 Bytes
0 to 255, +2 Bytes
14 Bytes
(2000 + 2) Bytes Max
B
R0 Record
Normal Record

Data Format (2314)



G0 = 45 bytes if R0 Data Length is 8 bytes
G0 = 45 + 0.043 (DL) if R0 Data Length 8 bytes
GN = 45 + 0.043 (KL + DL)

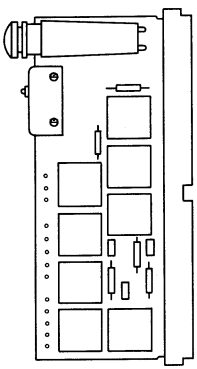
CE INDICATOR LATCH CARD

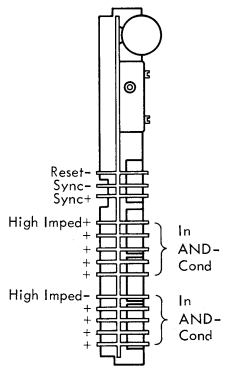
The CE indicator latch card part 5801358 can be used for two purposes:

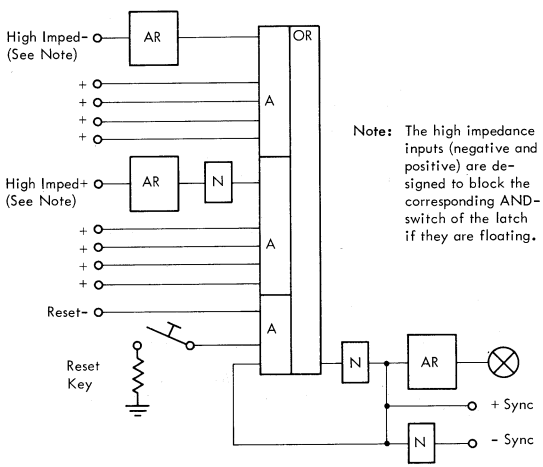
1. As a monitor to detect erroneous pulses and/or conditions.
2. As an AND switch to select a sync signal for a scope.

Note: Other CE indicator latch cards can be found in Tools and Test Equipment CEM #79. This CEM is on microfiche card CD102.

The latch on the card can be set by either negative or positive levels. A reset key is provided on the card so that the latch can be reset manually if desired. If the indicator latch card is to be used as an AND switch to select a certain sync signal for scoping, a reset signal must be provided to ensure correct triggering of the scope.







Note: The high impedance inputs (negative and positive) are designed to block the corresponding AND-switch of the latch if they are floating.

INTERRUPT CONDITIONS

I. Channel Working (SIO started and now working)

Exec. Inst.	CC	CSW Stored?	Comments
SIO any CU	2	No	No I/O opn starts
TIO any CU	2	No	No status transfers
HIO any CU	2	No	Irpts after halting current operation.
TCH	2	No	Status per CC (burst)

II. Channel End Pending *Channel Masked Off

*SIO any CU	2	No	Chan won't start I/O opn and will not clear the Irpt
TIO (to unit pending)	1	Yes	Clear Irpt store entire CSW
*TIO (other CU)	2	No	Chan untouched
HIO (any CU)	0	No	Chan stopped already
TCH	1	No	CC says Irpt pending

*Note: Dev End can be stacked back to device level on SIO, TIO (to other) so operation can start, CC = 0

III. Channel Clear Device End In Device

SIO (to unit 1 pending)	1	Yes (busy bit)	No I/O opn starts; Irpt is cleared
SIO (to other unit or dev)	0	No	I/O opn starts
TIO (to unit pending)	1	Yes	Irpt cleared
TIO (other unit or CU)	0	No	
HIO (any CU)	1	Yes	All Zero status
TCH	0	No	Under these conditions normally Device Poll Irpt

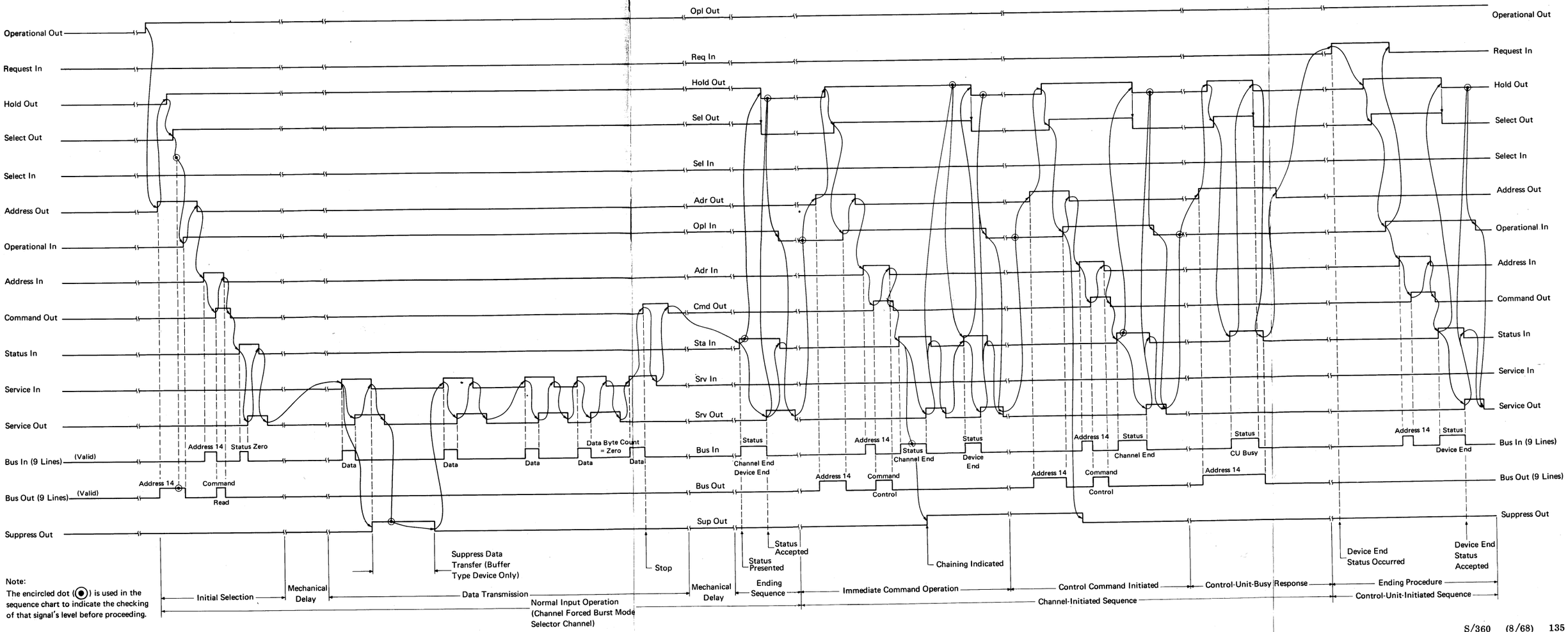
IV. Channel Clear but Irpt Pending in CU
(Dev End with other cond (unit check, etc)

SIO (unit pending)	1	Yes (busy bit)	No I/O opn starts, but clears Irpt
SIO (to other dev same CU)	1	Yes	Status says CU busy
SIO (other CU)	0	No	I/O opn starts
TIO (Device pending)	1	Yes	Clear Irpt
TIO (other dev same CU)	1	Yes (busy bit)	Status says CU busy
TIO (other CU)	0	No	

V. Polling Interrupt In Channel (No Irpt Response from CPU yet)

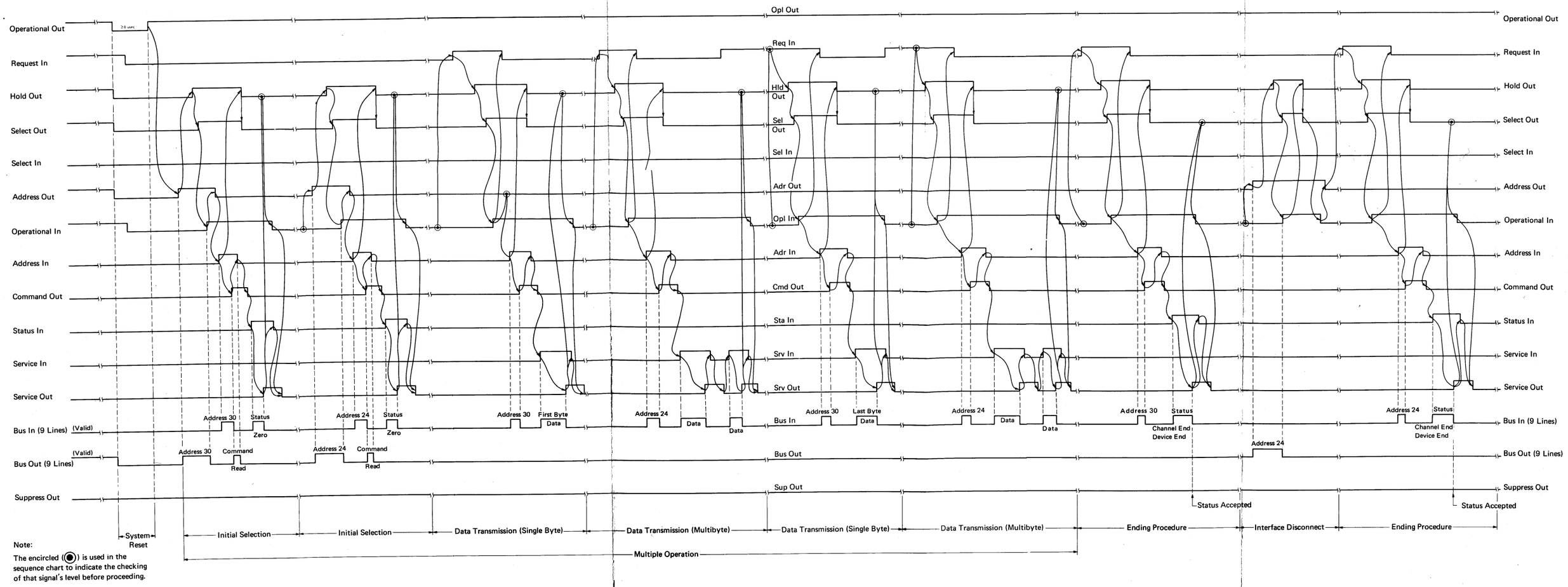
SIO, TIO, HIO } Any of these starting cause polled in status to be stacked back into the CU. (Command Out response to the Status In)

SELECTOR CHANNEL READ SEQUENCE

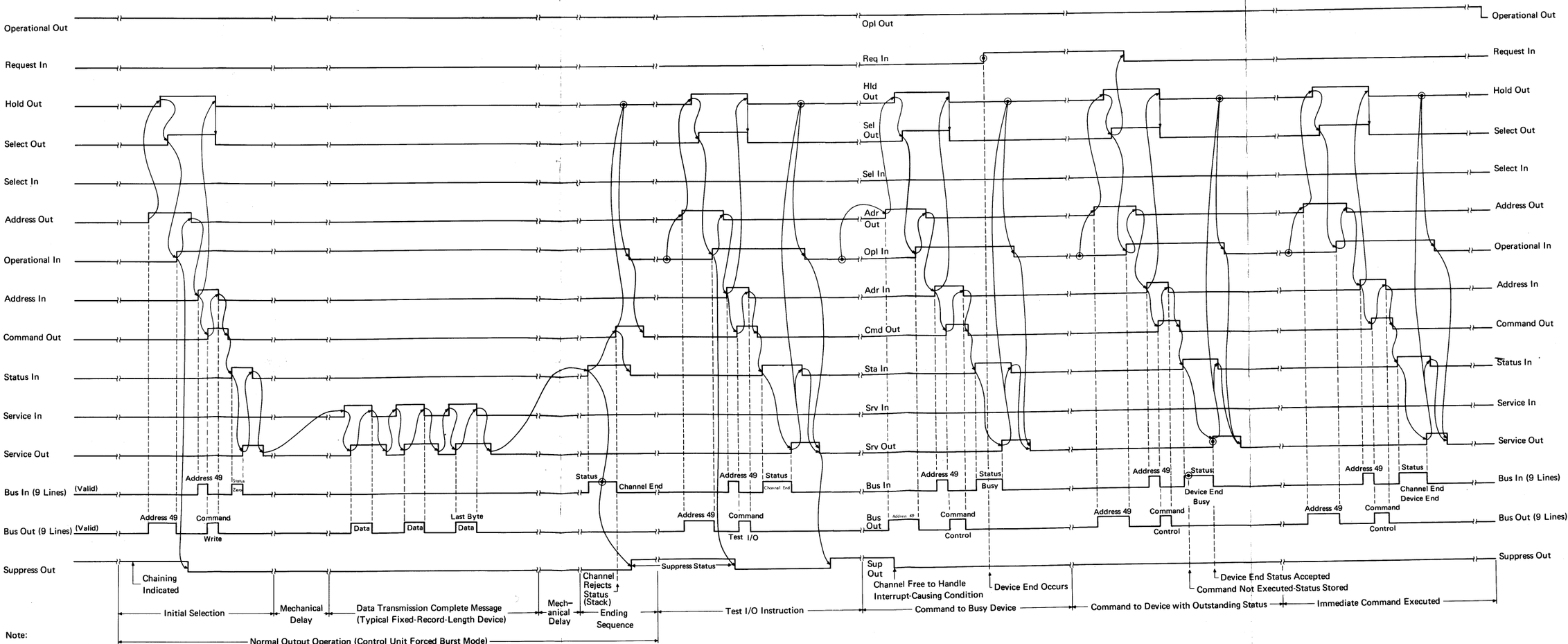


Note:
The encircled dot (◉) is used in the sequence chart to indicate the checking of that signal's level before proceeding.

MULTIPLEXER OPERATION

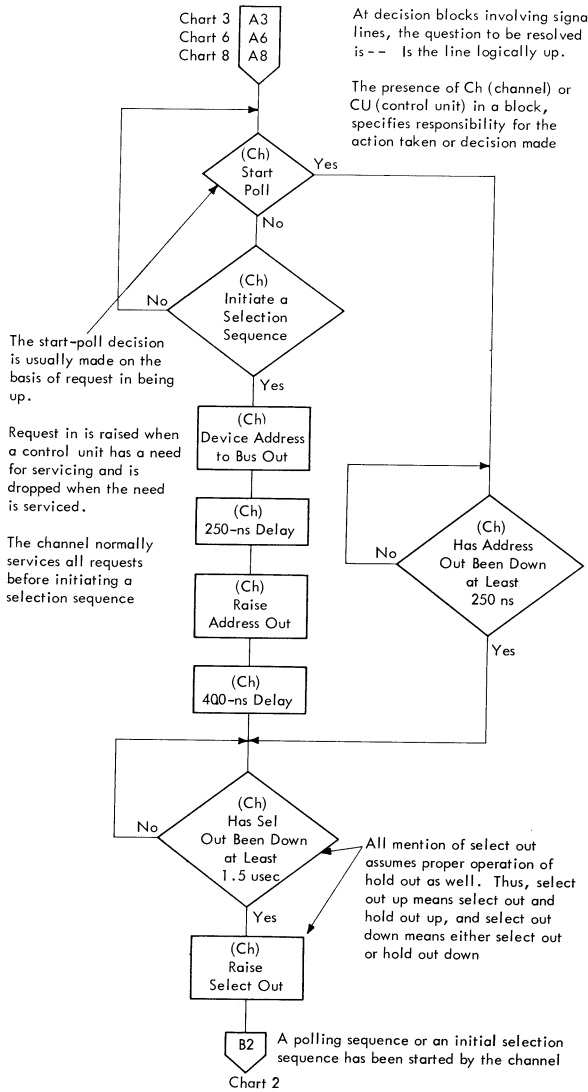


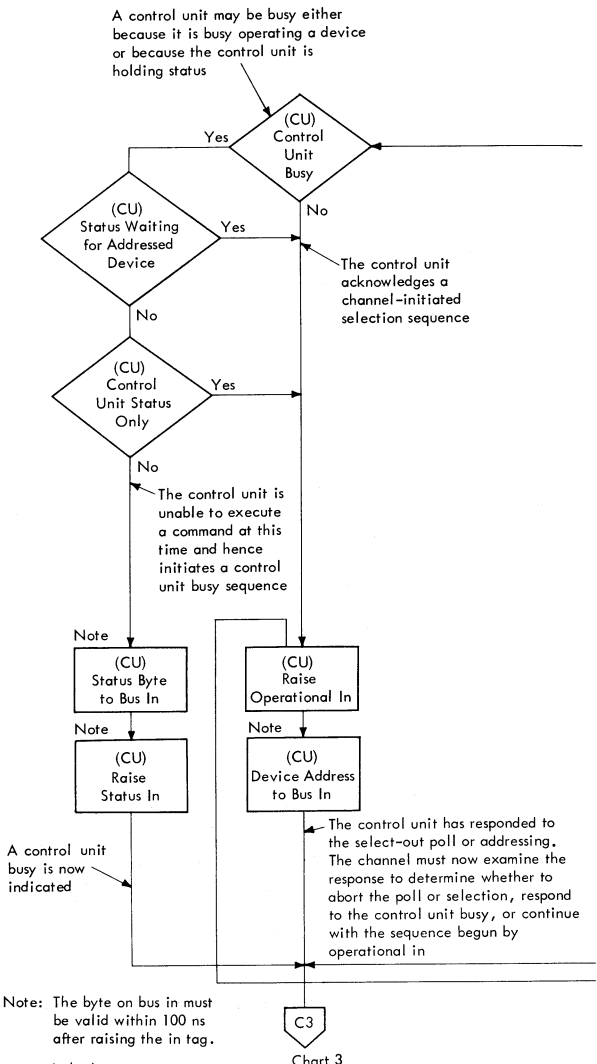
Note:
The encircled ((●)) is used in the sequence chart to indicate the checking of that signal's level before proceeding.



Note:
The encircled dot (◉) is used in the sequence chart to indicate the checking of that signal's level before proceeding.

Initiation of Polling or Selection -- Chart 1





Note: The byte on bus in must be valid within 100 ns after raising the in tag.

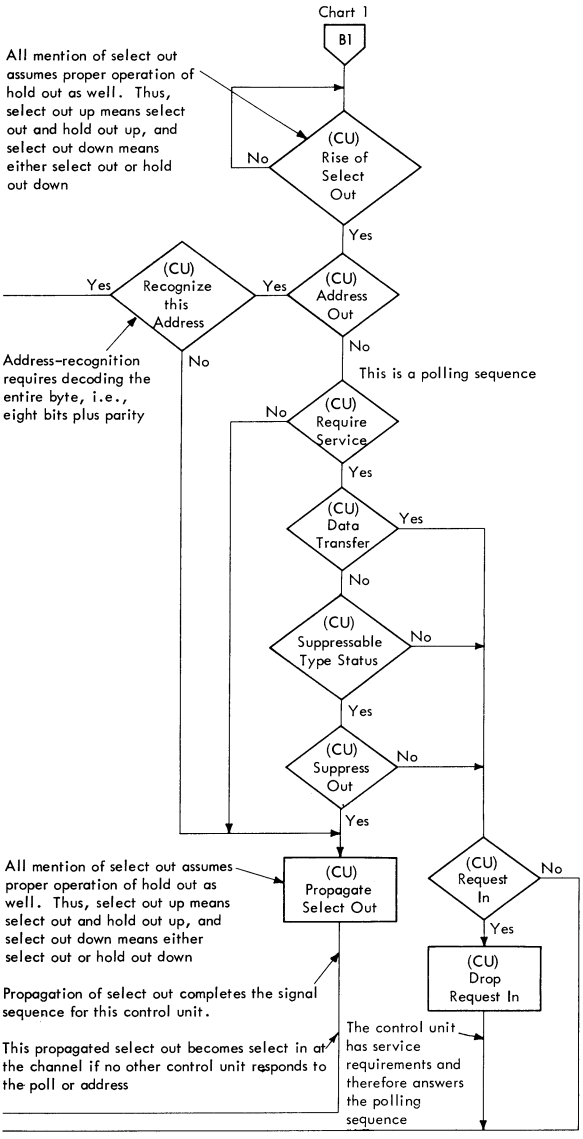
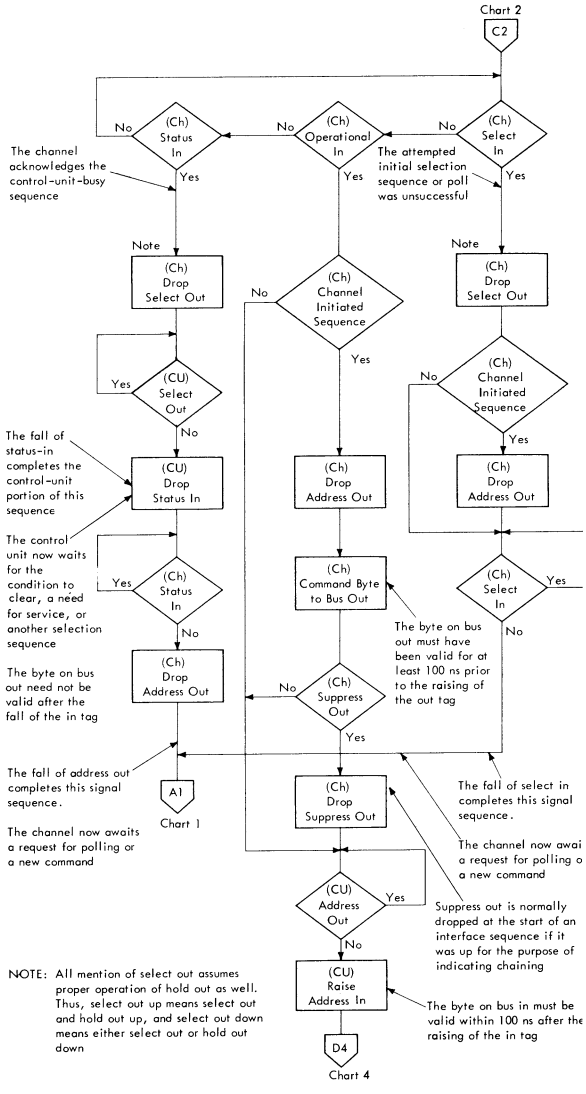
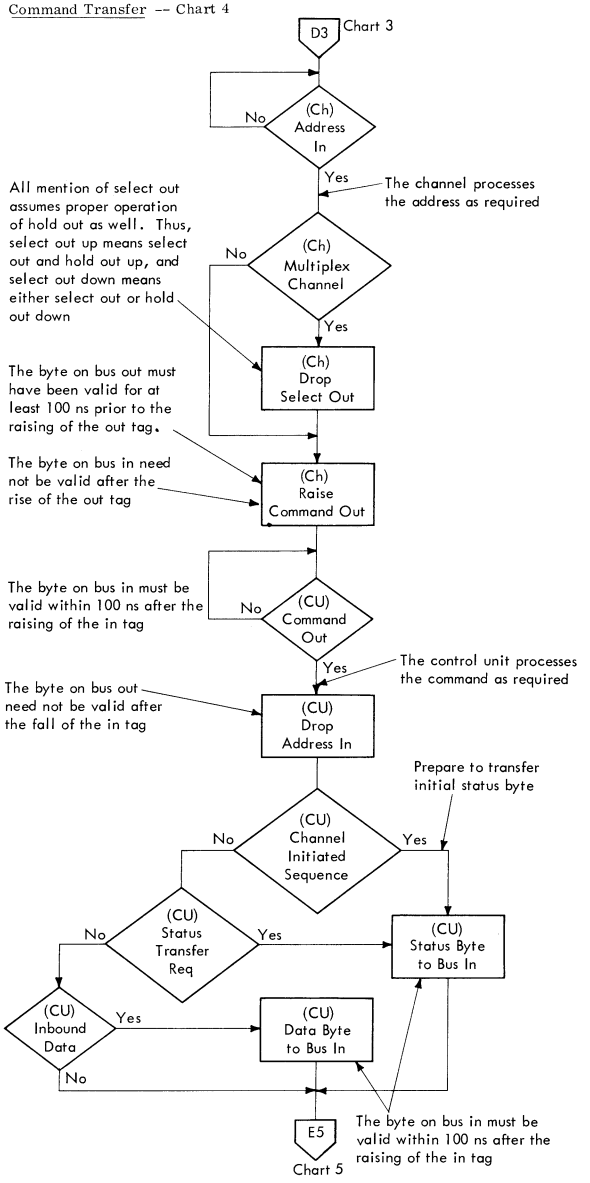
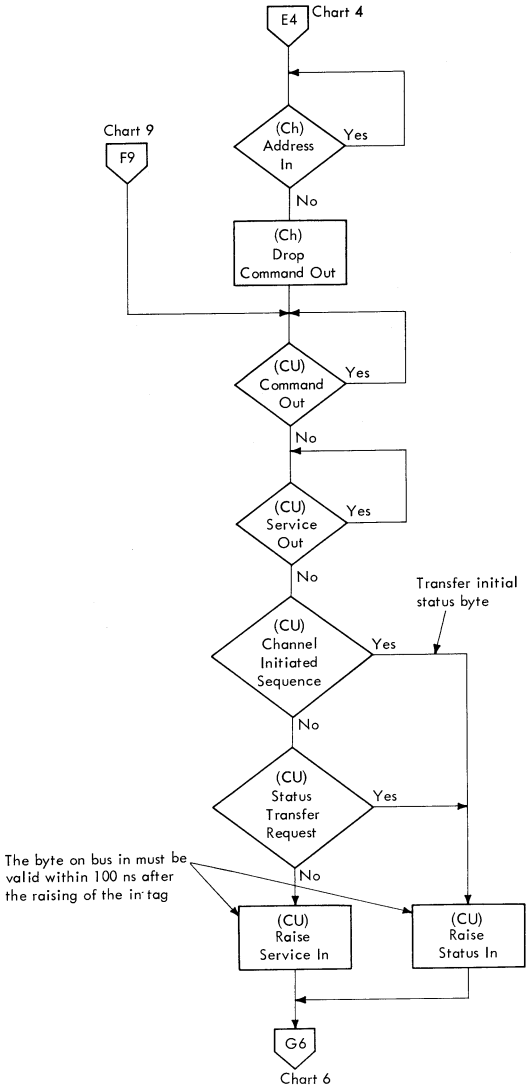


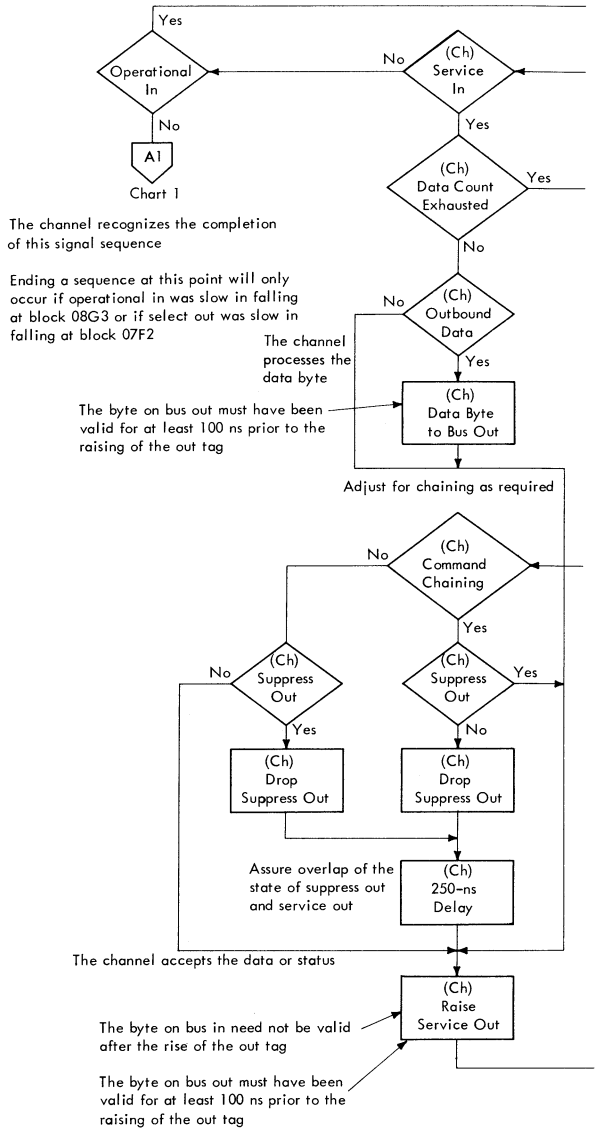
Chart 1
B1
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(CU) Rise of Select Out
No
Yes
(CU) Address Out
Yes
(CU) Recognize this Address
Yes
No
Address-recognition requires decoding the entire byte, i.e., eight bits plus parity
No
This is a polling sequence
(CU) Require Service
No
Yes
(CU) Data Transfer
Yes
No
(CU) Suppressable Type Status
No
Yes
(CU) Suppress Out
No
Yes
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(CU) Propagate Select Out
(CU) Request In
No
Yes
(CU) Drop Request In
Propagation of select out completes the signal sequence for this control unit.
This propagated select out becomes select in at the channel if no other control unit responds to the poll or address
The control unit has service requirements and therefore answers the polling sequence

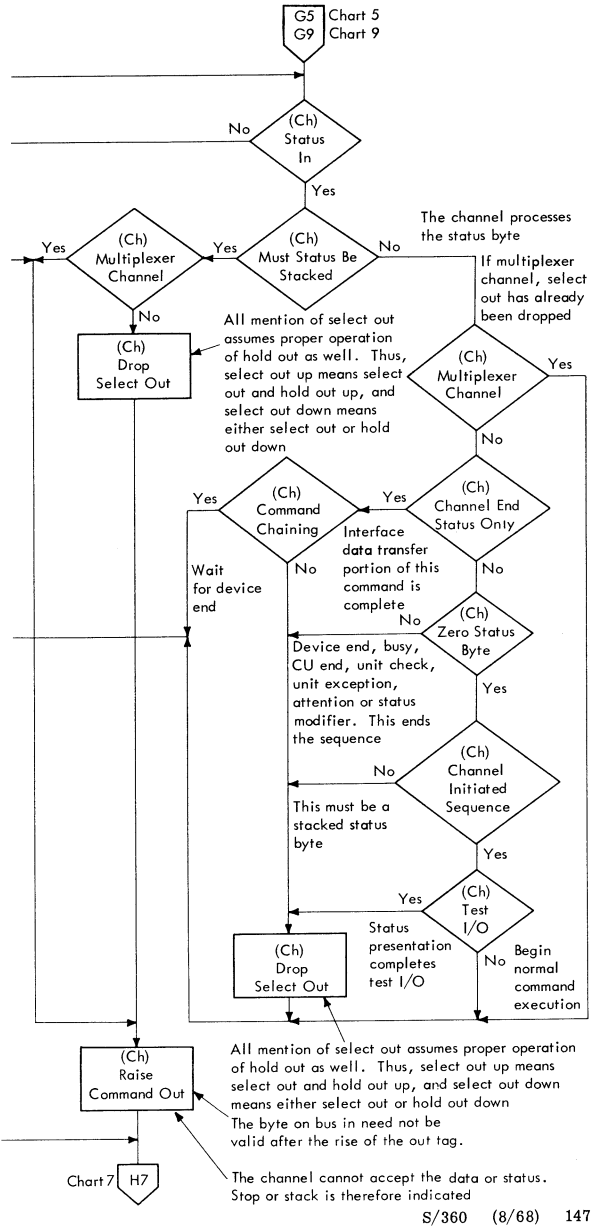


NOTE: All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down

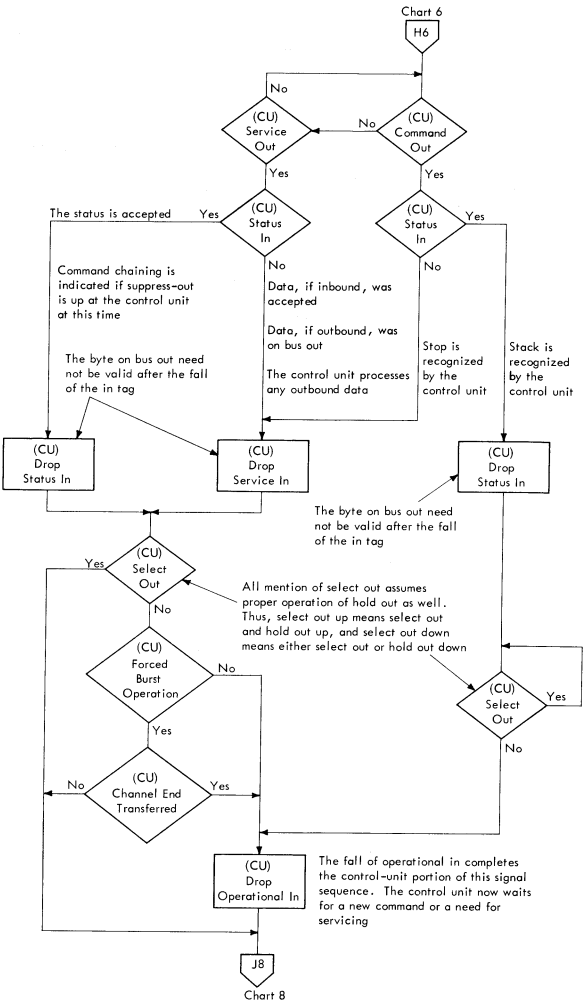

D3
Chart 3
(Ch) Address In
No
Yes
The channel processes the address as required
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(Ch) Multiplex Channel
No
Yes
(Ch) Drop Select Out
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag.
The byte on bus in need not be valid after the rise of the out tag
(Ch) Raise Command Out
The byte on bus in must be valid within 100 ns after the raising of the in tag
(CU) Command Out
No
Yes
The control unit processes the command as required
The byte on bus out need not be valid after the fall of the in tag
(CU) Drop Address In
Prepare to transfer initial status byte
(CU) Channel Initiated Sequence
No
Yes
(CU) Status Transfer Req
No
Yes
(CU) Status Byte to Bus In
(CU) Inbound Data
Yes
No
(CU) Data Byte to Bus In
E5
Chart 5
The byte on bus in must be valid within 100 ns after the raising of the in tag


E4
Chart 4
(Ch) Address In
Yes
No
Chart 9
F9
(Ch) Drop Command Out
(CU) Command Out
Yes
No
(CU) Service Out
Yes
No
Transfer initial status byte
(CU) Channel Initiated Sequence
Yes
No
(CU) Status Transfer Request
Yes
No
The byte on bus in must be valid within 100 ns after the raising of the in tag
(CU) Raise Service In
(CU) Raise Status In
G6
Chart 6


Yes
Operational In
No
No
(Ch) Service In
Yes
A1
Chart 1
(Ch) Data Count Exhausted
Yes
No
The channel recognizes the completion of this signal sequence
Ending a sequence at this point will only occur if operational in was slow in falling at block 08G3 or if select out was slow in falling at block 07F2
No
(Ch) Outbound Data
The channel processes the data byte
Yes
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag
(Ch) Data Byte to Bus Out
Adjust for chaining as required
No
(Ch) Command Chaining
Yes
No
(Ch) Suppress Out
(Ch) Suppress Out
Yes
Yes
No
(Ch) Drop Suppress Out
(Ch) Drop Suppress Out
Assure overlap of the state of suppress out and service out
(Ch) 250-ns Delay
The channel accepts the data or status
(Ch) Raise Service Out
The byte on bus in need not be valid after the rise of the out tag
The byte on bus out must have been valid for at least 100 ns prior to the raising of the out tag


G5 Chart 5
G9 Chart 9
No
(Ch) Status In
Yes
Yes
(Ch) Multiplexer Channel
Yes
(Ch) Must Status Be Stacked
No
The channel processes the status byte
If multiplexer channel, select out has already been dropped
No
(Ch) Drop Select Out
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(Ch) Multiplexer Channel
Yes
No
Yes
(Ch) Command Chaining
Yes
(Ch) Channel End Status Only
Wait for device end
No
Interface data transfer portion of this command is complete
No
(Ch) Zero Status Byte
Device end, busy, CU end, unit check, unit exception, attention or status modifier. This ends the sequence
Yes
No
(Ch) Channel Initiated Sequence
This must be a stacked status byte
Yes
Yes
(Ch) Test I/O
Status presentation completes test I/O
No
Begin normal command execution
(Ch) Drop Select Out
(Ch) Raise Command Out
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
The byte on bus in need not be valid after the rise of the out tag.
Chart 7 H7
The channel cannot accept the data or status. Stop or stack is therefore indicated

Response to Stack/Stop/Accept -- Chart 7



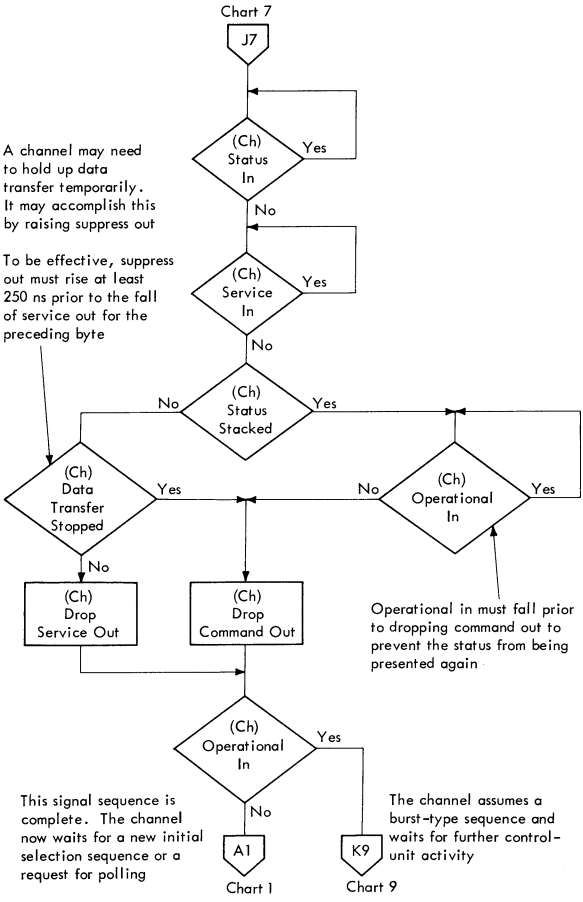


Chart 7
J7
(Ch) Status In
Yes
No
A channel may need to hold up data transfer temporarily. It may accomplish this by raising suppress out
To be effective, suppress out must rise at least 250 ns prior to the fall of service out for the preceding byte
(Ch) Service In
Yes
No
(Ch) Status Stacked
No
Yes
(Ch) Data Transfer Stopped
Yes
No
(Ch) Operational In
Yes
No
(Ch) Drop Service Out
(Ch) Drop Command Out
Operational in must fall prior to dropping command out to prevent the status from being presented again
(Ch) Operational In
Yes
No
This signal sequence is complete. The channel now waits for a new initial selection sequence or a request for polling
A1
Chart 1
The channel assumes a burst-type sequence and waits for further control-unit activity
K9
Chart 9

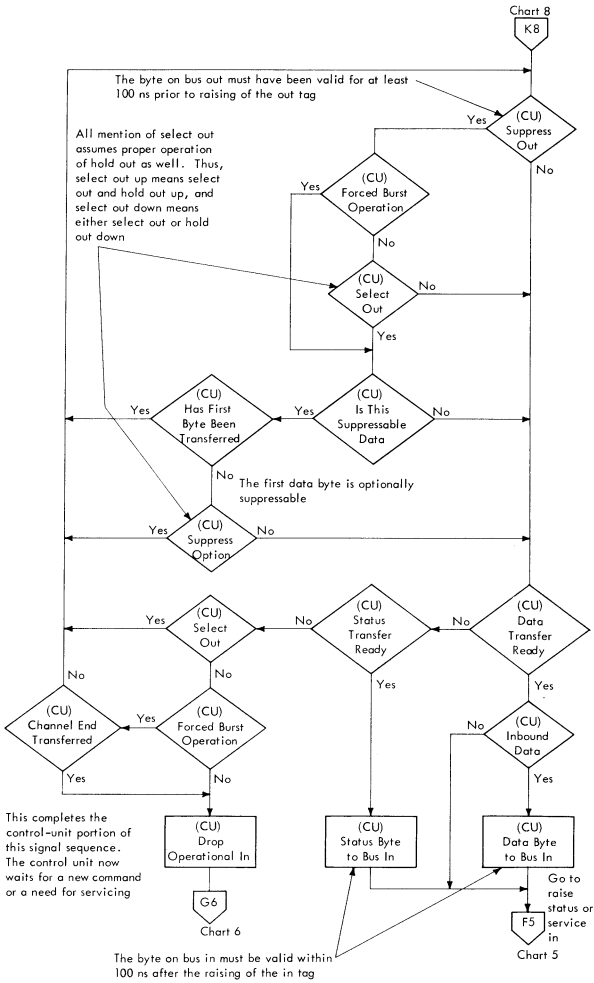
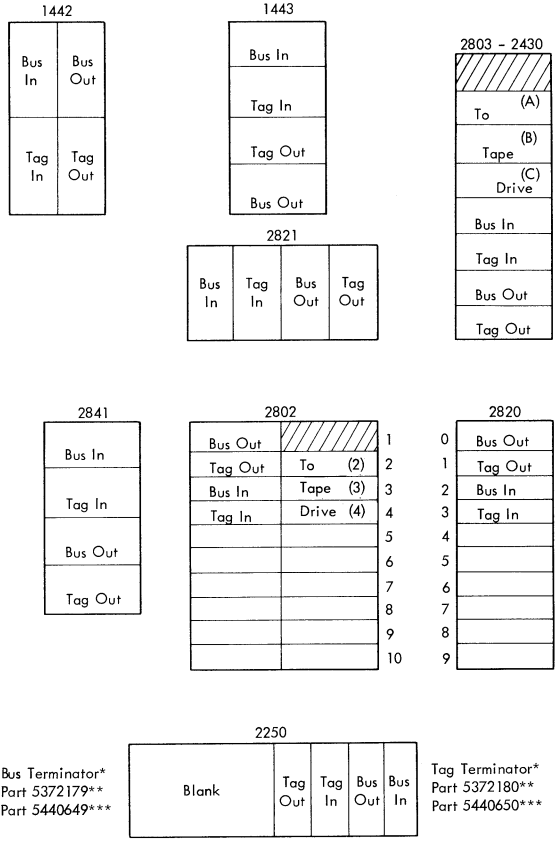


Chart 8
K8
The byte on bus out must have been valid for at least 100 ns prior to raising of the out tag
All mention of select out assumes proper operation of hold out as well. Thus, select out up means select out and hold out up, and select out down means either select out or hold out down
(CU) Suppress Out
Yes
No
(CU) Forced Burst Operation
Yes
No
(CU) Select Out
No
Yes
(CU) Has First Byte Been Transferred
Yes
(CU) Is This Suppressable Data
Yes
No
No
The first data byte is optionally suppressable
(CU) Suppress Option
Yes
No
(CU) Select Out
Yes
(CU) Status Transfer Ready
No
(CU) Data Transfer Ready
No
No
Yes
Yes
(CU) Channel End Transferred
No
(CU) Forced Burst Operation
Yes
(CU) Inbound Data
No
Yes
Yes
No
This completes the control-unit portion of this signal sequence. The control unit now waits for a new command or a need for servicing
(CU) Drop Operational In
(CU) Status Byte to Bus In
(CU) Data Byte to Bus In
G6
Chart 6
Go to raise status or service in
F5
Chart 5
The byte on bus in must be valid within 100 ns after the raising of the in tag

INTERFACE CONNECTORS



Note:
* Applies to all devices
** Before I/O Interface EC
*** After I/O Interface EC

Interface Connector Chart

	B	D	Connector 1	Connector 2
2	○	○		
3	•	+3V	Bus Out P	Operational In
4	○	•	Bus Out 0	Status In
5	•	○	Bus Out 1	Address In
6	-3V	•	Bus Out 2	Service In
7	○	○		
8	•	○	Bus Out 3	Select In
9	○	•	Bus Out 4	Select Out
10	•	○	Bus Out 5	Address Out
11	+6V	•	Bus Out 6	Command Out
12	•	○	Bus Out 7	Suppress Out
13	○	•		Service Out

	G	J	Connector 1	Connector 2
2	○	○		
3	•	+3V	Bus In P	Clock Out
4	○	•	Bus In 0	Metering Out
5	•	○	Bus In 1	Metering In
6	-3V	•	Bus In 2	Request In
7	○	○		
8	•	○	Bus In 3	
9	○	•	Bus In 4	
10	•	○	Bus In 5	
11	+6V	•	Bus In 6	
12	•	○	Bus In 7	Hold Out
13	○	•		Operational Out

CUT ALONG DOTTED LINE

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Suggested Addition (page___) Suggested Deletion (page___) Error (page___)

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